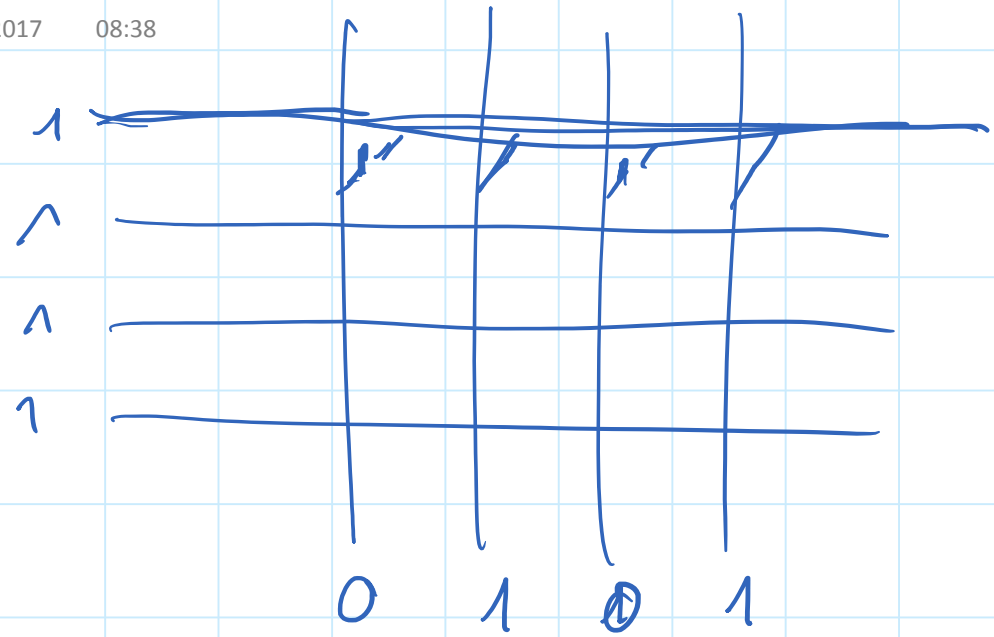
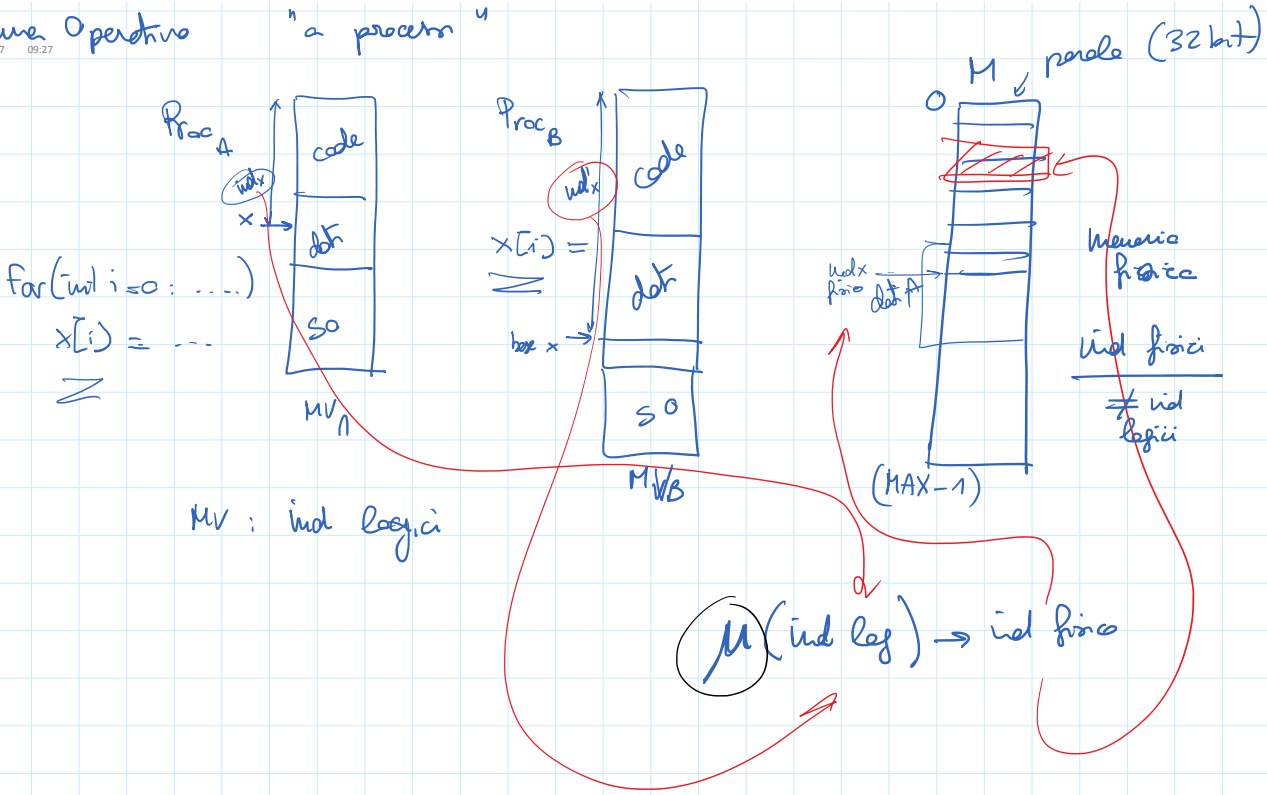
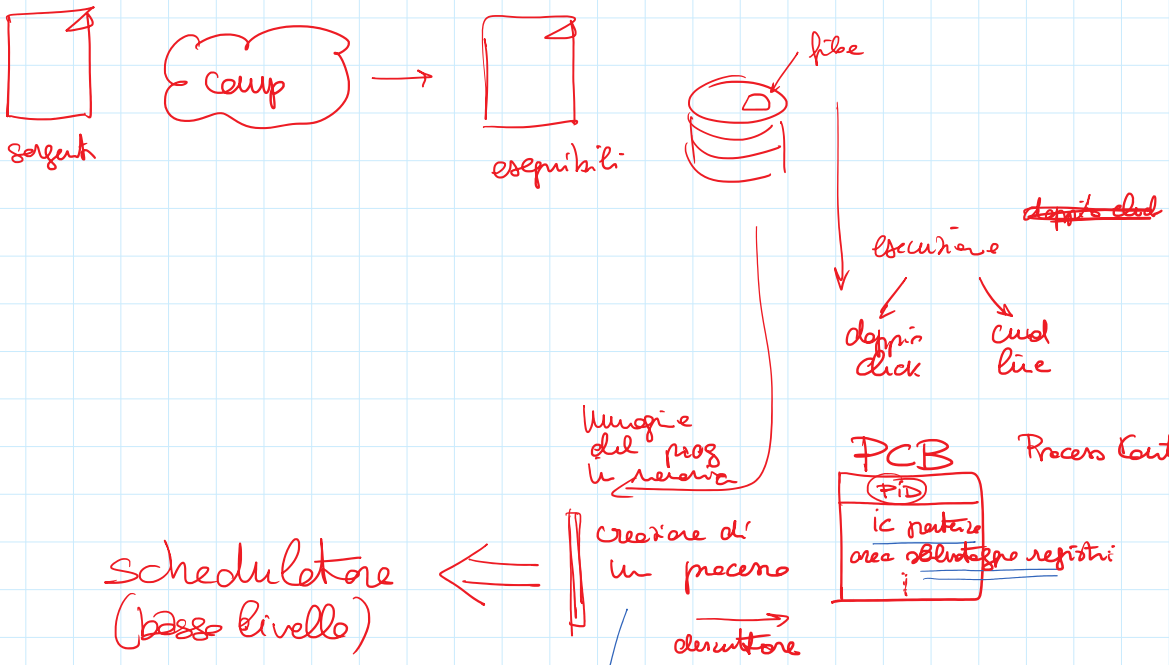
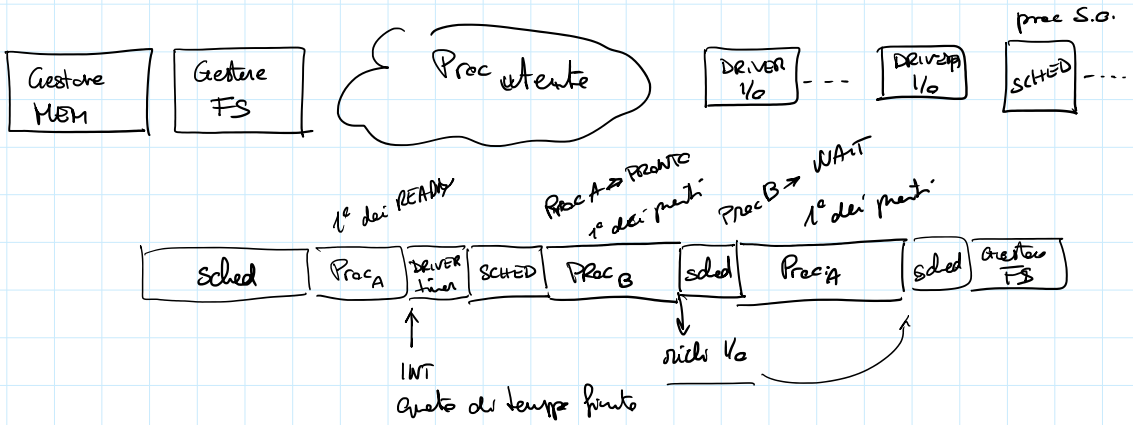
lunedì 13 novembre 2017 08:38

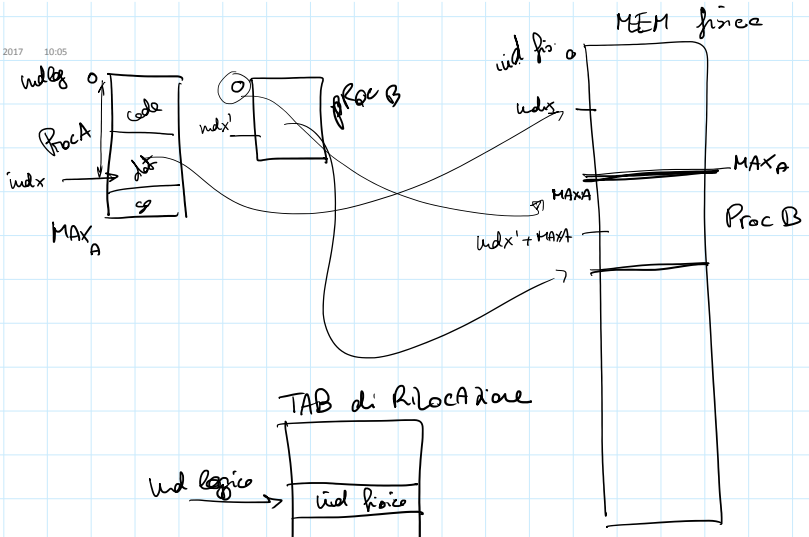


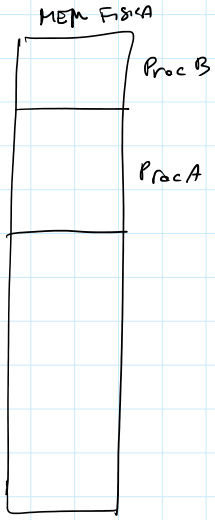
Sistema Operativo "a processi"

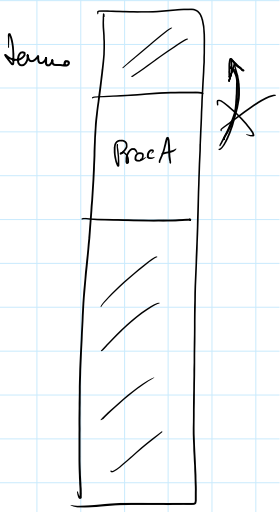


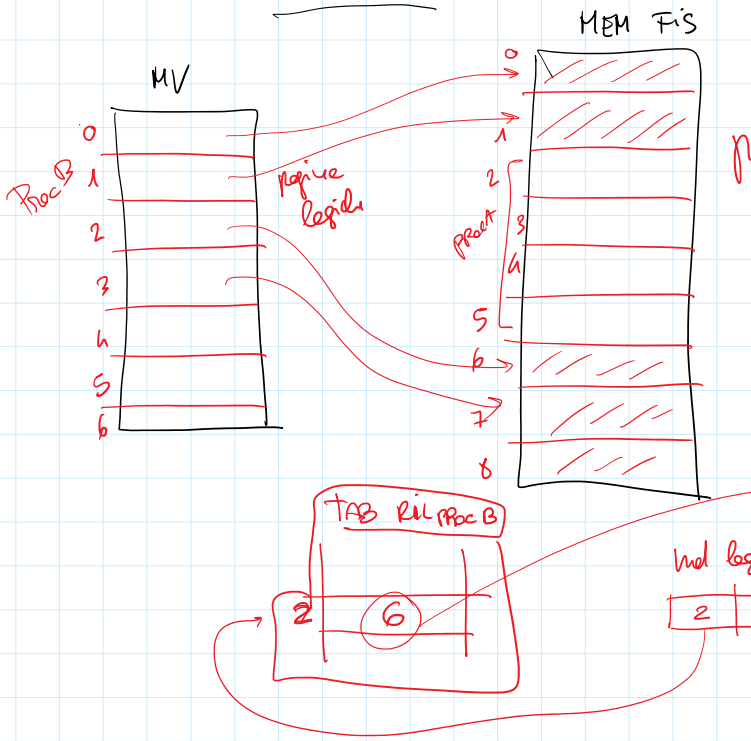



Gestore MEM
Gestore FS
Proc utente
DRIVER I/O
DRIVER I/O
SCHED
proc S.O.
1° dei READY
Proc A → PRONTO
1° dei pronti
Proc B → WAIT
1° dei pronti
sched
Proc A
DRIVER timer
SCHED
Proc B
sched
Proc A
sched
Gestore FS
INT
quota di tempo finita
richi I/o





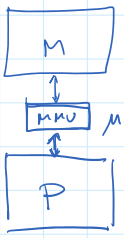




Indirizzo della TAB RIL è contenuto nel PCB

ind logico

D-RISC START_PROCESS Ric, Rtabril, Rtaglitabril



REG[Ric] → ic, REG[tabril] → int memoria della MMU

MASKINT Rmascheramento

EI enable interrupt

DI disable interrupt

bit di Rmascheramento è a 1 ⇒ int di tipo i non accettate altrimenti si ignorano

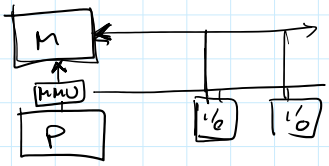
LD Rbase, Rindice, Rdest, DI

DI disable interrupt

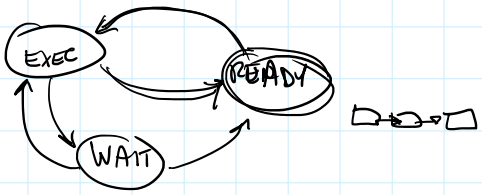
LD R_{base}, R_{indice}, R_{dest}, DI

SET_INDIV
RESET_INDIV
} hanno effetto su M

} set indiv
LOAD
STORE
} reset indiv



COPY_IC R_{reg} IC → REG[regg]



Commuta contesto:

Ⓐ proc exec → salvato → ready

Ⓑ 1° della lista ready → exec

Proc A

Ⓐ

STORE $R_{base\ PCB}$, $R_{area\ salvataggio}$, R_1

INC R

STORE " " , R_2

...

Copy_ic

...

PCB mio nella lista dei pronti

Ⓑ 1° prendere il 1° PCB nella lista dei pronti

PCB_B

LOAD

LOAD

LOAD

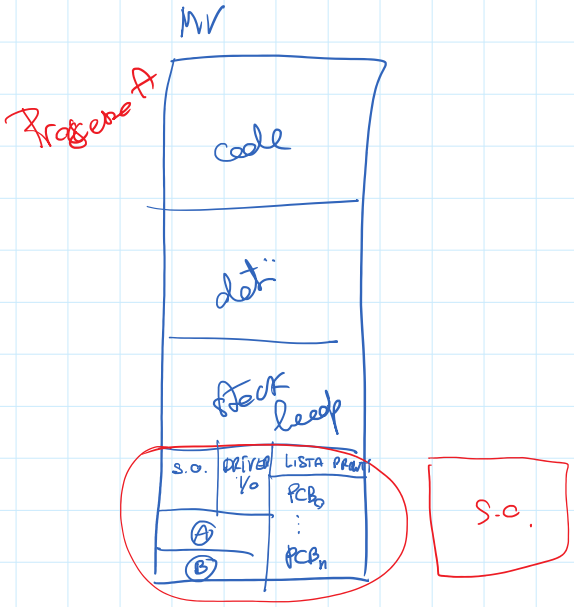
...

Area di salvataggio

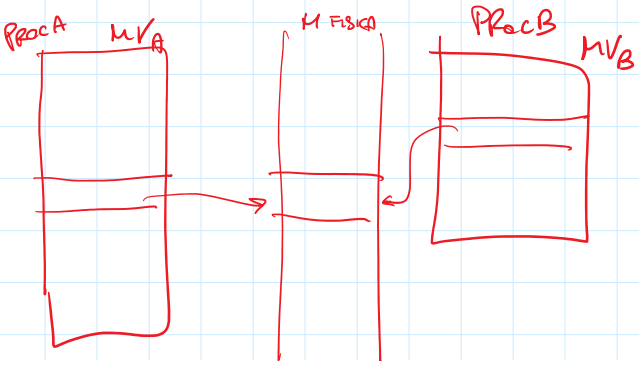
registri "stato salvato"

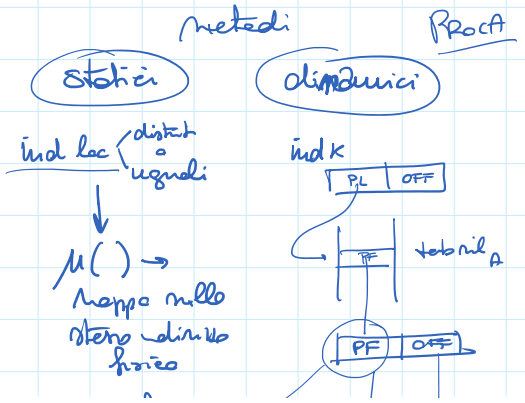
F

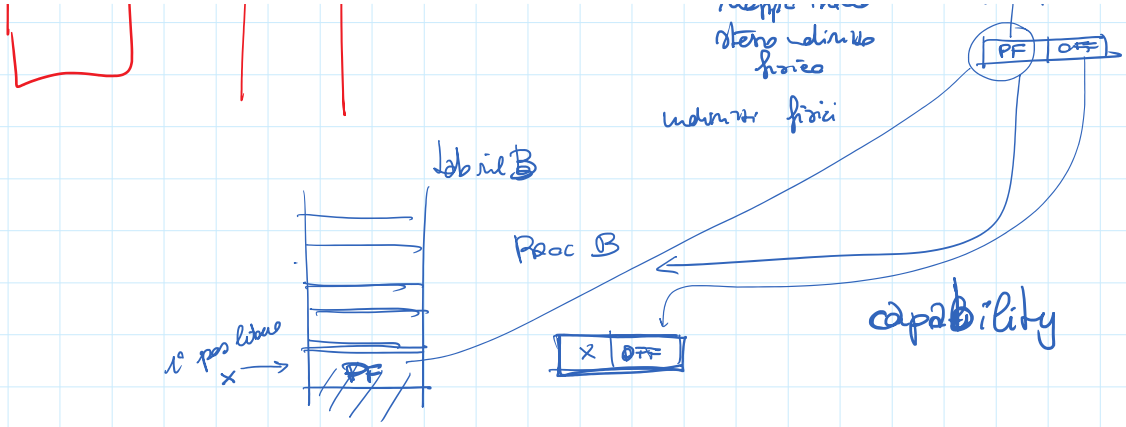
START_PROCESS R_{ic}, $R_{labiril}$



2 processi distinti accedono allo stesso indirizzo in memoria centrale






PF
OFF
tab ind B
Proc B
1° pos libera
x
X
OFF
capability