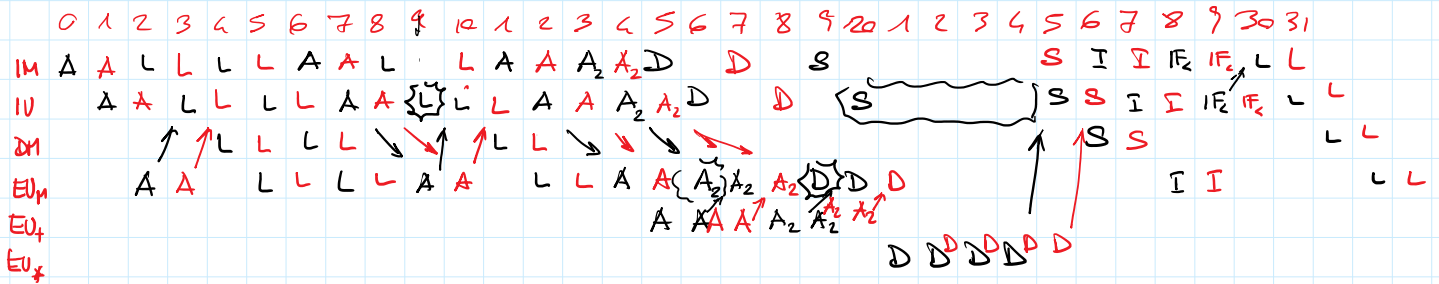


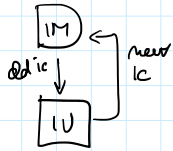
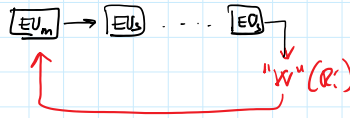
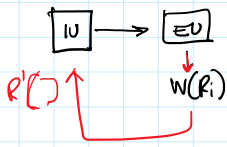
```

Loop: 1 ADD Ri, #-1, Ri-1
      2 LOAD RbaseA, Ri-1, R1
      3 LOAD RbaseA, Ri, R2
      4 ADD Ri, #1, Ri+1
      5 LOAD RbaseA, Ri+1, R3
      6 ADD R2, R3, R4
      7 ADD R1, R4, R5
      8 DIV R5, #3, R6
      9 STORE RbaseB, Ri, R6
     10 INC Ri
     11 HZ Ri, Rv, loop
    
```

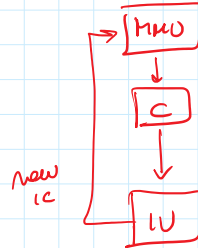
$$T = \frac{30t}{22}$$



DIP LOCICHE



SACTI



	0	1	2	3	4	5
MMU	IF ₂					
C		IF ₂				
IM			IF ₂	X	X	target

```
for(i=0; i<2N; i++) {
    x[i] = i;
}
```

```
for(i=0; i<2N; i++) {
    x[i] = i;
    i++;
    x[i] = i;
}
```

```
loop: STORE R_base, R_i, R_i;
      INC R_i;
      STORE R_base, R_i, R_i;
      INC R;
      IF2 R_i, R_2N, loop;
```

```
CLEAR (R_i)
loop: STORE R_base, R_i, R_i;
      INC R_i;
      IF2 R_i, R_2N, loop;
```

	0	1	2	3	4	5	6	7	8	9	10	11
IM	st	inc	IF ₂	X	X							
IU		st	inc	IF ₂	IF ₂	X	st					
DM			st					st				
EU _m				inc								

$$T = \frac{5t}{3}$$

IM	st	inc	st	inc	IF ₂	X	st		
IU		st	inc	st	inc	IF ₂	IF ₂	X	st
DM			st						st
EU _m				inc		inc			

$$T = \frac{8t}{6}$$

~~loop: STORE R_base, R_i, R_i;
 INC R_i;
 INC R_i;
 IF₂ R_i, R_2N, loop;
 STORE R_base, R_i, R_i;~~

```
loop: STORE R_base, R_i, R_i;
      ADD R_i, #1, (R_1)
      ADD R_i, #2, R_i;
      IF2 R_i, R_2N, loop, delayed;
      STORE R_base, R_1, R_1;
```

IM	st	A ₁	X ₂	IF ₂	IF ₂	st	st
IU		st	A ₁	A ₂	IF ₂	IF ₂	st
DM			st				st
EU				A ₁	X ₂		

A ↔ A

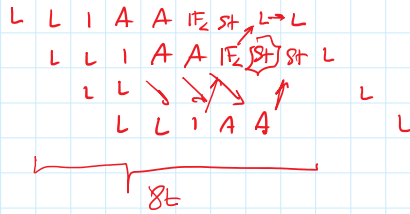
IM
IU
DM
EU

```
STORE ---
ADD R_i, #2, R_i;
SUB R_i, #1, R_i;
IF del
STORE ---
```

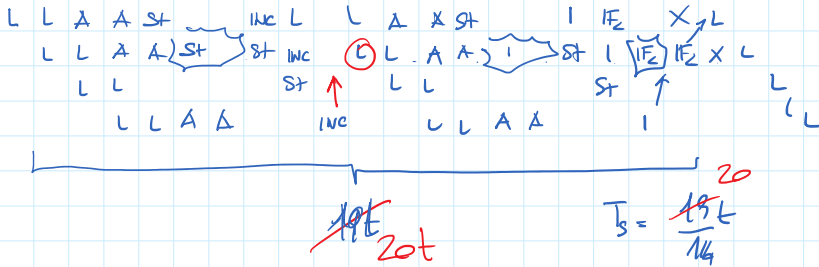
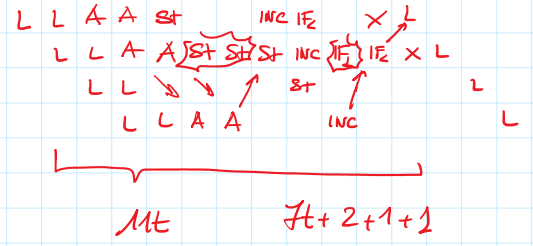
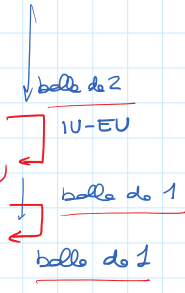
for(i=0; i<2N; i++)
 x[i] = a[i] + b[i] + *;

loop
 LOAD
 LOAD
 ADD
 ADD
 STORE
 INC
 LOAD
 LOAD
 ADD
 ADD
 STORE
 INC
 IFZ

loop
 LOAD
 LOAD
 INC
 ADD
 ADD
 IFZ *delayed*
 STORE *delayed* R_{base} + i, R₄

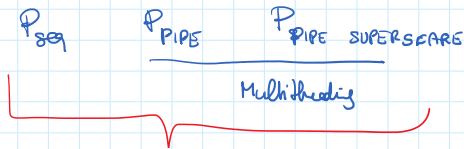


loop:
 LOAD R_{base}, R₁, R₁
 LOAD R_{base} + b, R₁, R₂
 ADD R₁, R₂, R₃
 ADD R₃, R₄, R₄
 STORE R_{base} + x, R₁, R₄
 INC R₁
 IFZ R₁, R_{2N}, loop



MULTICORE

mercoledì 13 dicembre 2017 10:15

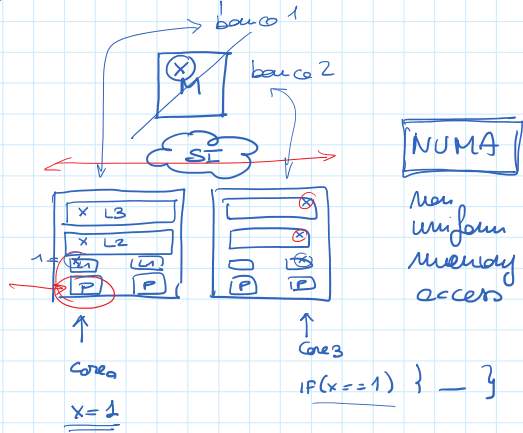


replicazione di componenti del processore

Multicore

architettura o memoria condivisa

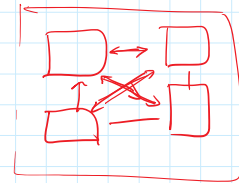
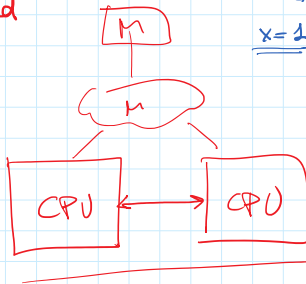
replicazione del P



cache coherence

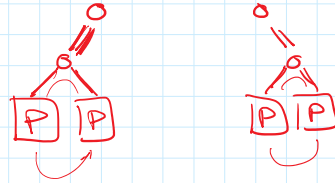
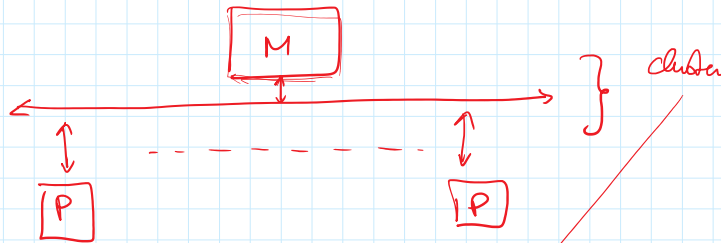
Snoopy based

directory based

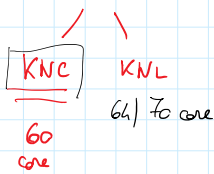


Multiprocessore Simmetrico

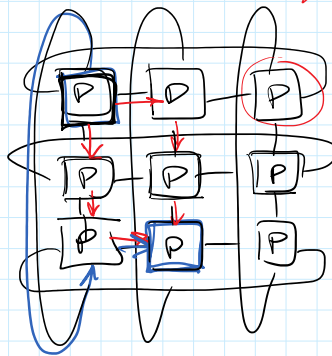
FAT TREE



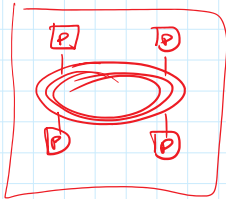
Xeon Phi



MESH

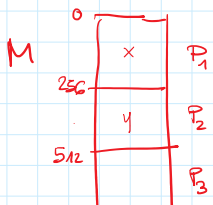


Dark silicon



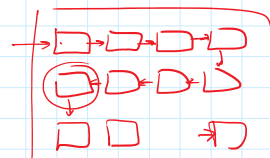
PAAS

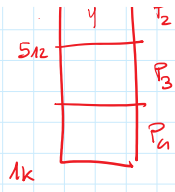
Partitioned Global Address Space



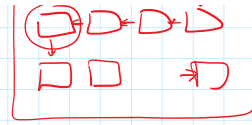
Epiphany V

1024
S1 Mesh

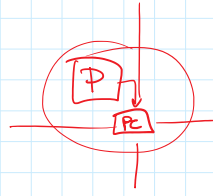




1024
S1 Mesh



\sqrt{n}



CELL IBM

