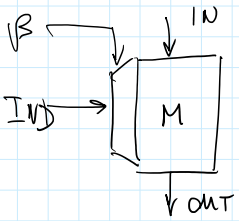
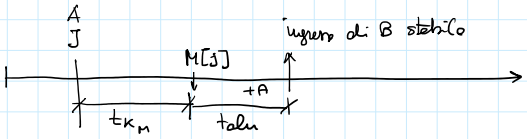
Memorie nelle PO (ritardi)

lunedì 16 ottobre 2017 09:14

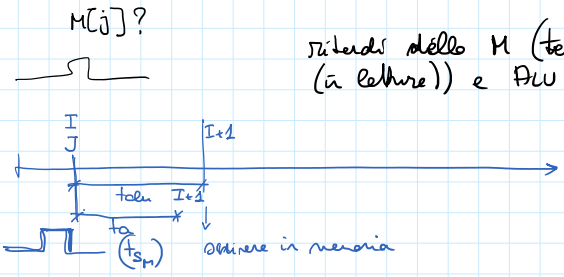


Lettura di una memoria $M[j] + A \rightarrow B$

Scrittura in una memoria $I+1 \rightarrow M[j]$



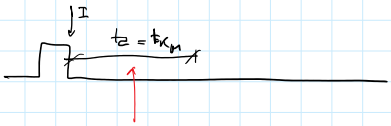
GPO



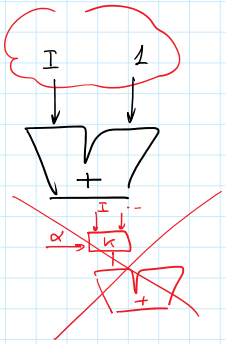
Ritardi della M (tempo di accesso (in lettura)) e ALU si sommano

UPO

$(M[I]_{\emptyset} = {}^{0}_{1}?)$

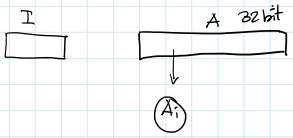


$(M[I+1]_0 = {}^{0}_{1}?)$



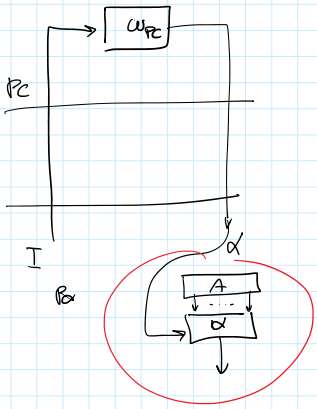
Controllo residuo

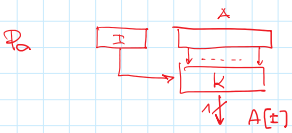
lunedì 16 ottobre 2017 09:30



$\emptyset$. $(I = 0)$ $A_0 \to B$
$(= 1)$ $A_1 \to B$
$(= 2)$ $A_2 \to B$
$\vdots$
$(= 31)$ $A_{31} \to B$

$\log_2 32 = 5$
non dipende da

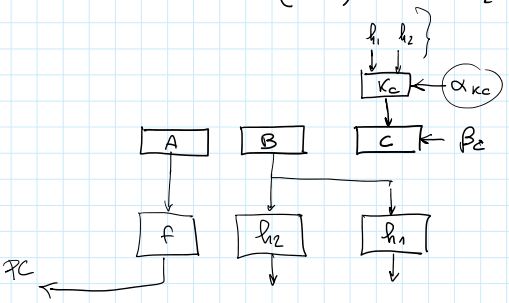




se $(f(A) = 0)$ $h_1(B) \to C$
else $h_2(B) \to C$

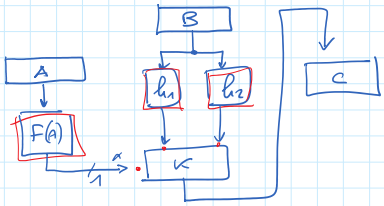
F, h_1 e h_2 sono funzioni pure quindi rete combinatoria

$\emptyset$. $(f(A) = 0)$ $h_1(B) \to C$, 1.
$(= 1)$ $h_2(B) \to C$, 1.



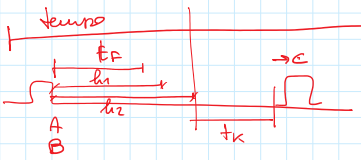
1ª fase del processo fornela di abilitazione PB

2ª fase del processo " " " "



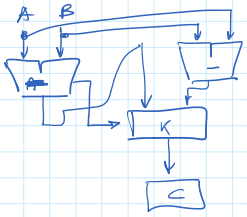
t_F t_{h_1} t_{h_2}

$\max\{t_F, t_{h_1}, t_{h_2}\} + t_K$

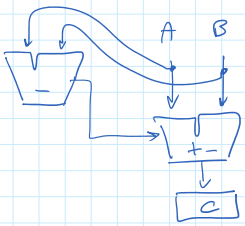


IF $(A > B)$ $A \to B \to C$
else $B \to A \to C$

$\emptyset$. $(\text{segno}(A - B) = \emptyset)$ $A - B \to C$, 1
$(= 1)$ $B - A \to C$, 1



$\emptyset$. $(\text{segno}(A - B) = 0)$ $A - B \to C$, 1
$(= 1)$ $A + B \to C$, 1



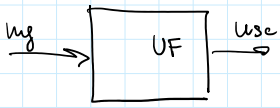
fatto con controllo residuo

1) 

2) $\emptyset$. $A \to B \to C \big|_{\text{segno}(A-B)=0}$, $A + B \to C \big|_{\text{segno}(A-B)=1}$

tempi di elaborazione

lunedì 16 ottobre 2017 09:55



{ op esterne } $\#m$

k_i è il # delle μ-istruzioni eseguite x calcolare op-est_i

μ-programma (di controllo) $\Rightarrow$

op est$_0$ k_0

⋮

op est$_{m-1}$ k_{m-1}

PO (sintesi con comp. standard)

PC (sintesi classica ($\omega_{PC}, \sigma_{PC}, R$))

τ

$T = \sum_{i=0}^{m-1} p_i k_i \tau$

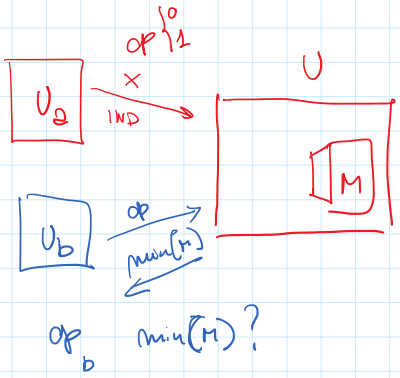
tempo medio di elaborazione

$p_i \in (0,1)$

p_i è la prob che venga richiesto op-est$_i$

τ → ottimizzazione vuol dire trovare PO/PC + veloci nel singolo ciclo di clock

k → ottimizzazione vuol dire trovare un sequenza con un minor numero di μ-istruzioni che implenta la op esterna



op_b min(M) ?

op = 0

x → M[IND] ← 1 μ-istruzione

op = 1

cerco ∀x in M e la cambio x/8192

ciclo x scorrere M
fissare che mio M[I] == x ?
fissare x/8192

Ciclo x scorrere M
fissare x capire min (M[I], min)

1024
2048

Interazioni

U_a, U_b } dandare a U che è pronto a rispondere

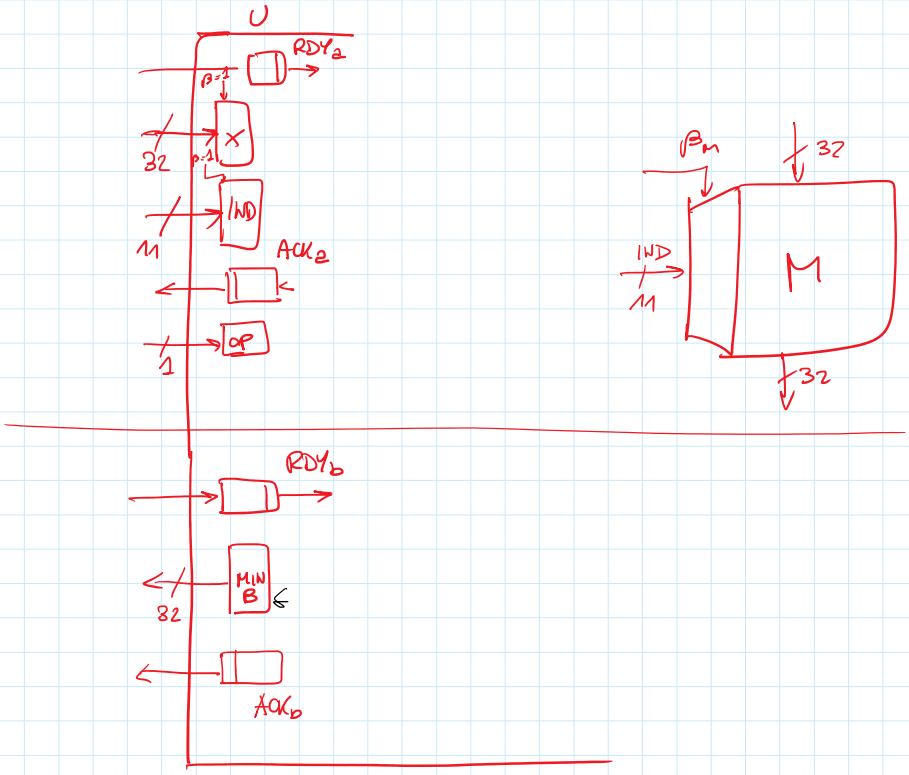
↓

necessità di una politica x U per rispondere in caso di richiesta multiple (sia U_a che U_b)

{ fissa / fair

Interfacce

$U_a \leftrightarrow U$



$U_b \leftrightarrow U$

priorità all'unità U_b

$\emptyset$. $(RDY_a, RDY_b = 00)$ map, $\emptyset$
$(=10)$ "serve U_a"
$(=01)$ "serve U_b"
$(=11)$ "serve U_b"

M 2K pos

$\frac{2^{32}-1}{2^{31}-1}$

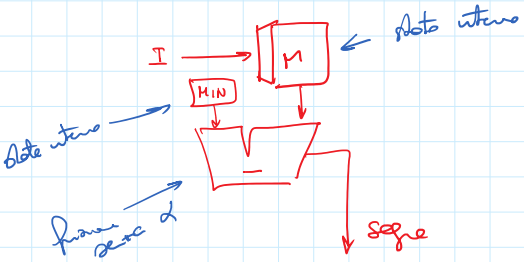
$\emptyset$ $(RDY_a, RDY_b=0)$ map, $\emptyset$
$(=-1)$ "serve U_b" ⟶
$(=10)$ "serve U_A"

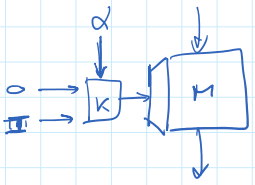
M[0] → MIN
1 → I
i (finito? min?) <
= =

$\emptyset$. $(=-1)$ M[0] → MIN, 1 → I, 1 (I: 12 bit)

1. $(I_0, segno(MIN - M[I]) = 00)$ M[I] → MIN, I+1 → I, 1.
$(=01)$ I+1 → I, 1
$(=1-)$ MIN → MINB, set Ack_b, reset RDY_b, $\emptyset$

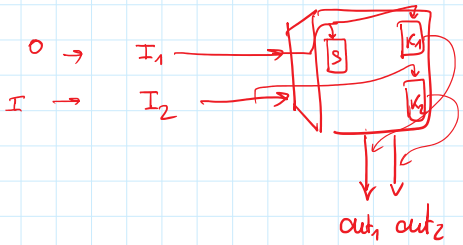
uscite verso la PC





Violazione della condizione di correttezza

M "a doppio porto"



0. $(RDY_a, RDY_b = 00)$ nop $\emptyset$
   $(= -1)$ $M[0] \to MIN$, $1 \to I$, 1
   $(= 10)$ nop, 2
1. ....
2. $(OP = 0)$
   $(= 1)$

$\emptyset$. $(RDY_a, RDY_b, OP = 00-)$ nop, $\emptyset$
   $(= -1-)$ $M[0] \to MIN$, $1 \to I$, 1
   $(= 100)$ $X \to M[IND]$, set ACK_a, reset RDY_A, $\emptyset$
   $(= 101)$ $\emptyset \to \overset{12\ bit}{I}$, 2
1. ....
2. $(I_0, zero(X - M[I]) = 00)$ $I+1 \to I$, 2
   $(= 01)$ $X/8192 \to M[I]$, $I+1 \to I$, 2
   SHR(X, 13)
   $(= 1-)$ set ACK_a, reset RDY_A, $\emptyset$

τ ? π ?