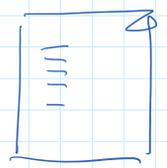


Modelli di costo

$$T_{id} + \underbrace{\text{costo (fault di cache)}}_{\neq}$$

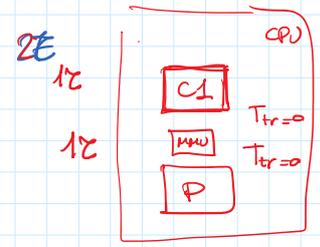


.D RISC

$$T_c = \underbrace{a}_\downarrow t_1 + \underbrace{b}_\downarrow t_2$$

$$T_c = 100t_1 + 90t_2$$

cache 1° livello comune x dati e prog  
di tipo exec. in univ.  $t_2$  ? in caso di bit



$$T_c = 100t_1 + 90(2t_2)$$

tempo di completamento ideale

costo del trattamento dei fault

$\# \text{ fault} \cdot (\text{costo del singolo fault})$

WS

↓  
dipende dal codice  
(e in parte dall'hw)

↓  
dipende dall'hw

↖  
Coproctor



| PL | OFF |

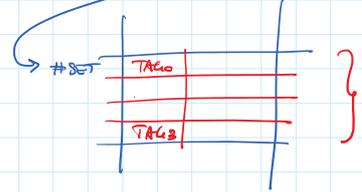
IND LOG → IND FIS. CI

| PL | OFF |

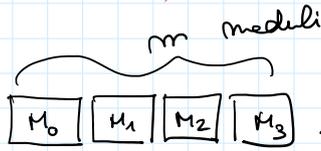
(PAG?)



IND di CACHE  
(MOD di IND)



# $T_{\text{fault}}$ ( $T_{\text{test}}$ )



interallocati

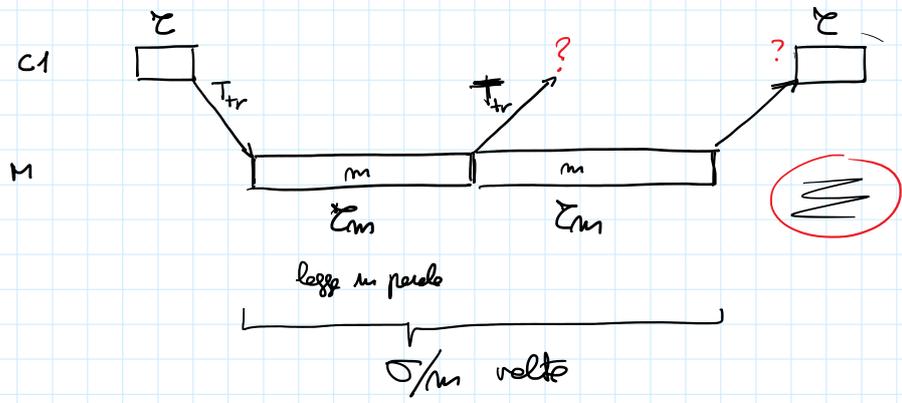
non avere/utilizzare il  $k$  che "sceglie" fra i moduli

?  
Cosa è il  $\sigma$  e l'interfaccia



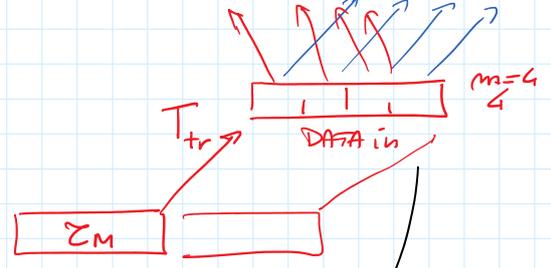
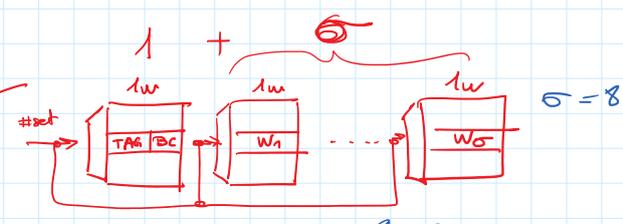
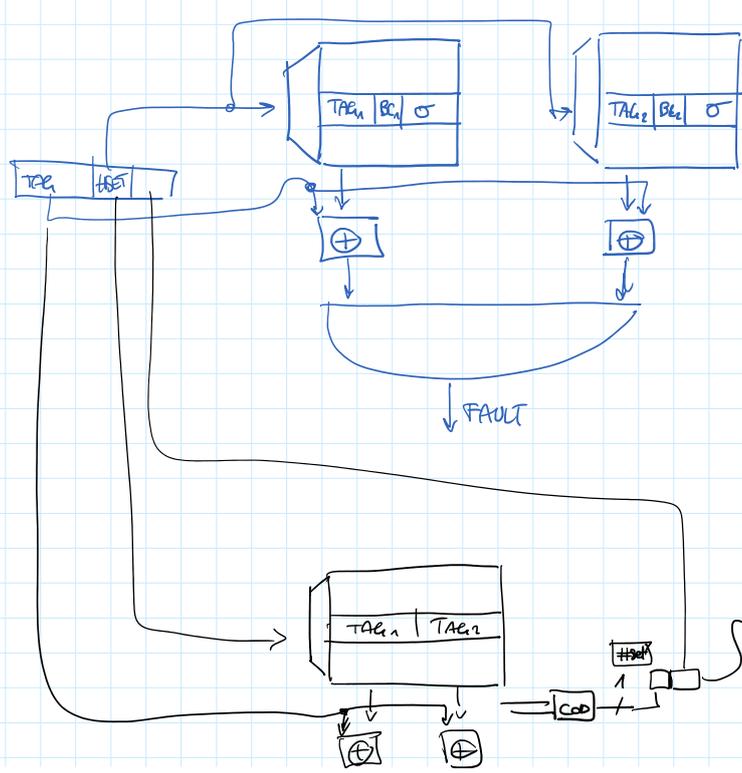
interfaccia con reg DATA IN DATA OUT da  $\frac{\sigma}{m}$  parole

$T_{\text{fault}} \propto \frac{\sigma}{m}$



$(2T_{tr} + 2\sigma) + \frac{\sigma}{m} \Sigma_m$

set associativo a 2 vie



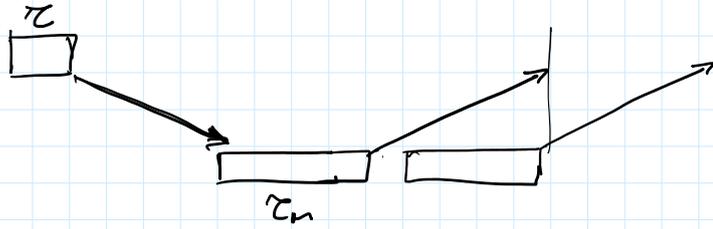
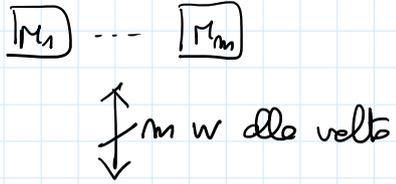
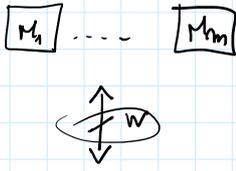
$m \Sigma$  cicli

\_\_\_\_\_

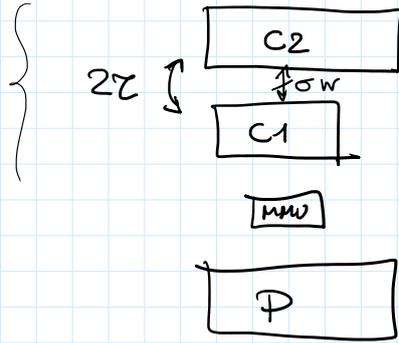


\_\_\_\_\_

\_\_\_\_\_



$$T_{fault} \propto \frac{g}{m} \quad \frac{g}{m} T_{tr}$$

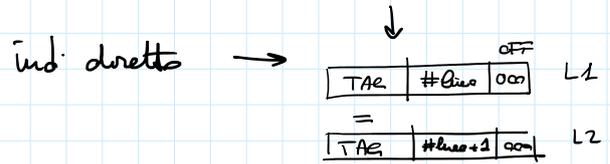


$\sigma_2 \neq \sigma_1$        $\sigma_2 > \sigma_1$        $\sigma_2 = 16$   
 $\sigma_1 = 8$

credito  $(C1 - C2)$  ?

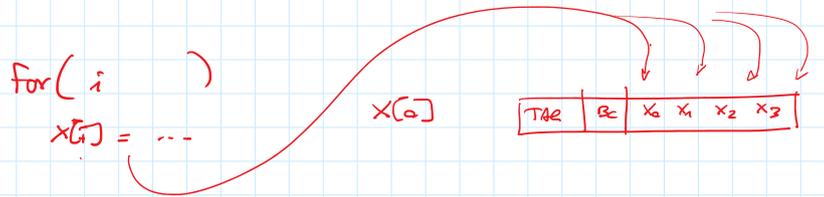
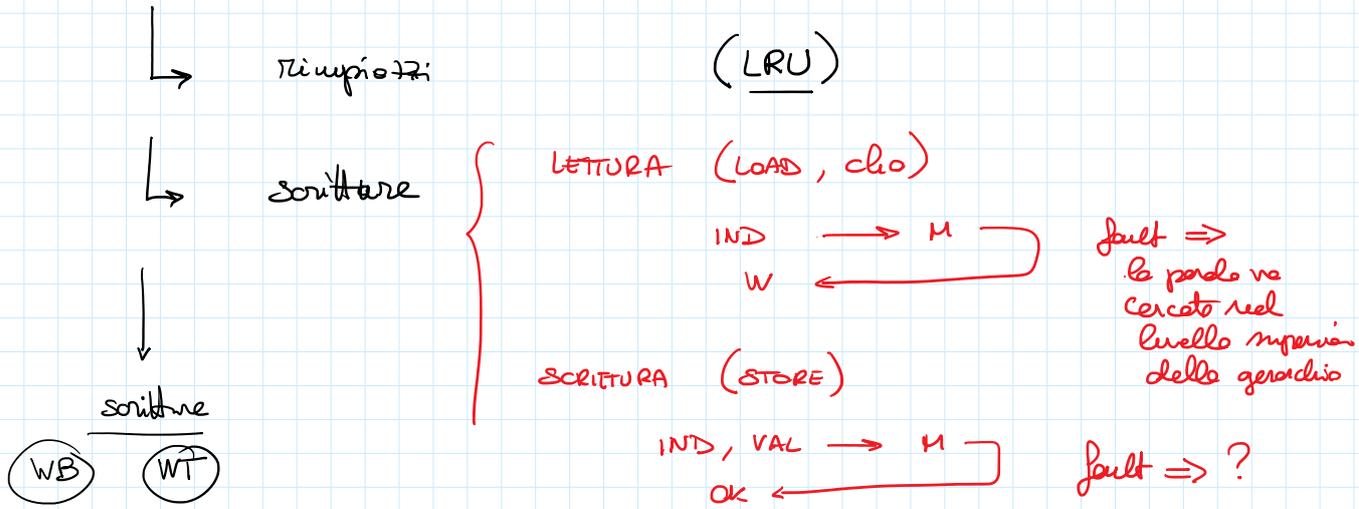
se accedo L1 in C1  
 è probabile che accedo a L2  
 subito dopo

L2 è "consecutivo" a L1



$$T_c = T_{id} + \#fault \cdot T_{fault}$$

### Politiche di gestione delle cache



```
for(i=0; i<N; i++)
    x[i] = f(y[i])
```

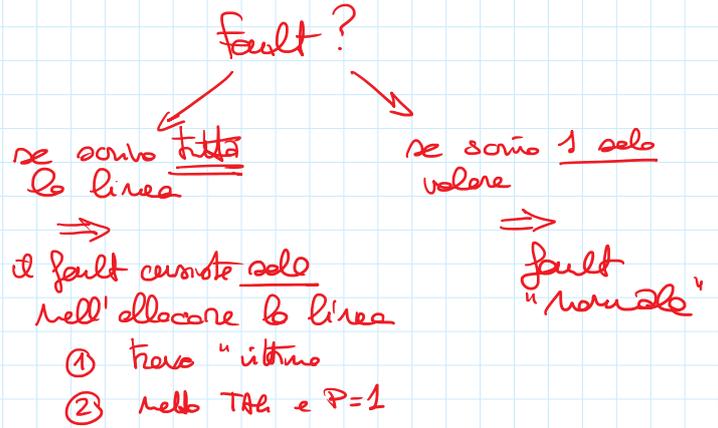
#fault ?

$$\frac{\#istr}{\sigma} + \frac{2N}{\sigma}$$

$$T_c = T_{id} + \#fault \cdot T_{fault}$$

↑  
 $\frac{\#istr}{\sigma} + \frac{1N}{\sigma}$

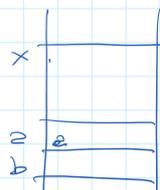
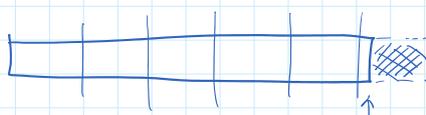
x che non considero le scritte



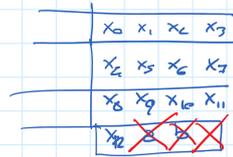
hp1 vettore x "allineato" alle linee di cache



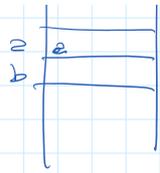
hp2 padding x l'ultimo linee di cache



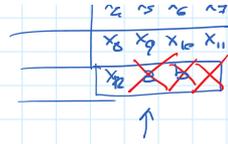
} int x[13];  
 float a, b;



σ=4



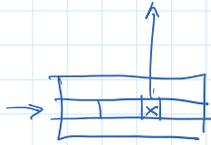
font e, b;



# WRITE BACK

✓ scrittura deve essere riportata al livello superiore

scrittura asincrona



P STORE  $i_d, x$

- 1) ricevo lo indirizzo di STORE
- 2) scrivo in C e ordino lo scritto in P
- 3) do risposta (esito) al P

```
for (i )
    x[i] = i;
```

```
for: STORE Rbase, Ri, Ri
    INC Ri
    IFZ Ri, Rn, for
END
```

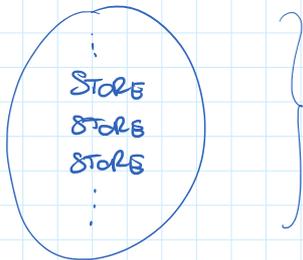
write back

$T_c$  di 1 iterazione

$$3 \begin{pmatrix} cl_0 + cl_1 \\ 2\tau + t_2 \end{pmatrix} + \begin{pmatrix} T_{store} + T_{inc} + T_{ifz} \\ 2\tau + t_2 \quad 1\tau \quad 2\tau \end{pmatrix}$$

$$6\tau + 3t_2 + 5\tau + t_2 \Rightarrow 11\tau + 4t_2$$

$\downarrow$   
 $8\tau$   
 $\underbrace{\hspace{10em}}_{23\tau}$



# WRITE THROUGH

✓ scrittura avviene solo nel livello di cache considerato

+ quando la linea diventa "vittima" x multiplicità

⇒ ripeto l'iterazione nel livello superiore