1 RETI COMBINATORIE

giovedì 22 settembre 2016 14:09

Algebra di Boole

$\{F, T\}$ $\{0, 1\}$ $\{$AND $\cdot$, OR $+$, NOT $-\}$ binarie

2 bit → 1 bit

1 bit → 1 bit

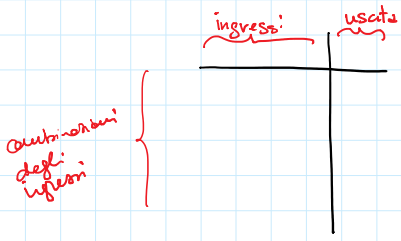
x bit

$\overline{x}$ NOT(x)

$x \,\&\, y$ = x AND y

$x \mid y$ = x OR y

Tabella di verità



n ingressi → 2^n righe

AND

x_1	x_2	z
0	0	0
0	1	0
1	0	0
1	1	1

OR

x_1	x_2	z
0	0	0
0	1	1
1	0	1
1	1	1

NOT

x	z
0	1
1	0

Conoscenza logica

$A + \overline{A} = 1$ $A\overline{A} = 0$

$\overline{\overline{A}} = A$

$A + A = A$ $A \cdot A = A$

A	A·A
0	0
1	1

$A + 0 = A$ $A \cdot 1 = A$

$A + 1 = 1$ $A \cdot 0 = 0$

$A + B = B + A$ $A \cdot B = B \cdot A$

$A + (B + C) = (A + B) + C$

$A(BC) = (AB)C$

$A(B + C) = AB + AC$

$A + BC = (A + B)(A + C)$

$\overline{A + B} = \overline{A} \cdot \overline{B}$ $\overline{AB} = \overline{A} + \overline{B}$

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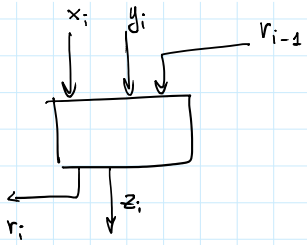
fun "addizionatore di due bit con riporto"



x_i	y_i	r_{i-1}	z_i	r_i
0	0	0	0	0
0	0	1	1	0
0	1	0	1	0
0	1	1	0	1
1	0	0	1	0
1	0	1	0	1
1	1	0	0	1
1	1	1	1	1

expr dei booleani

("forma canonica")
somma di prodotti

$$z_i = \bar{x}_i \cdot \bar{y}_i \cdot r_{i-1} + \bar{x}_i\, y_i\, \bar{r}_{i-1} + x_i\, \bar{y}_i\, \bar{r}_{i-1} + x_i\, y_i\, r_{i-1}$$

$$r_i = \bar{x}_i\, y_i\, r_{i-1} + x_i\, \bar{y}_i\, r_{i-1} + x_i\, y_i\, \bar{r}_{i-1} + x_i\, y_i\, r_{i-1}$$

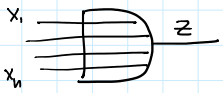
$\forall 1$ della colonna
$\rightarrow$ termine: prodotto degli ingressi negati se valgono ϕ nella riga
non negati " " 1 " "

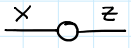
$$(x_i\, y_i)\,\bar{r}_{i-1} + (x_i\, y_i)\, r_{i-1} = x_i\, y_i\, (\bar{r}_{i-1} + r_{i-1}) = x_i\, y_i$$

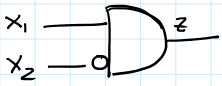
$(\bar{r}_{i-1} + r_{i-1}) = 1$

$$r_i = \bar{x}_i\, y_i\, r_{i-1} + x_i\, \bar{y}_i\, r_{i-1} + x_i\, y_i$$

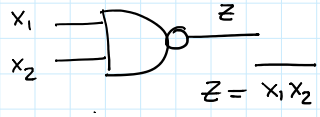
AND OR NOT





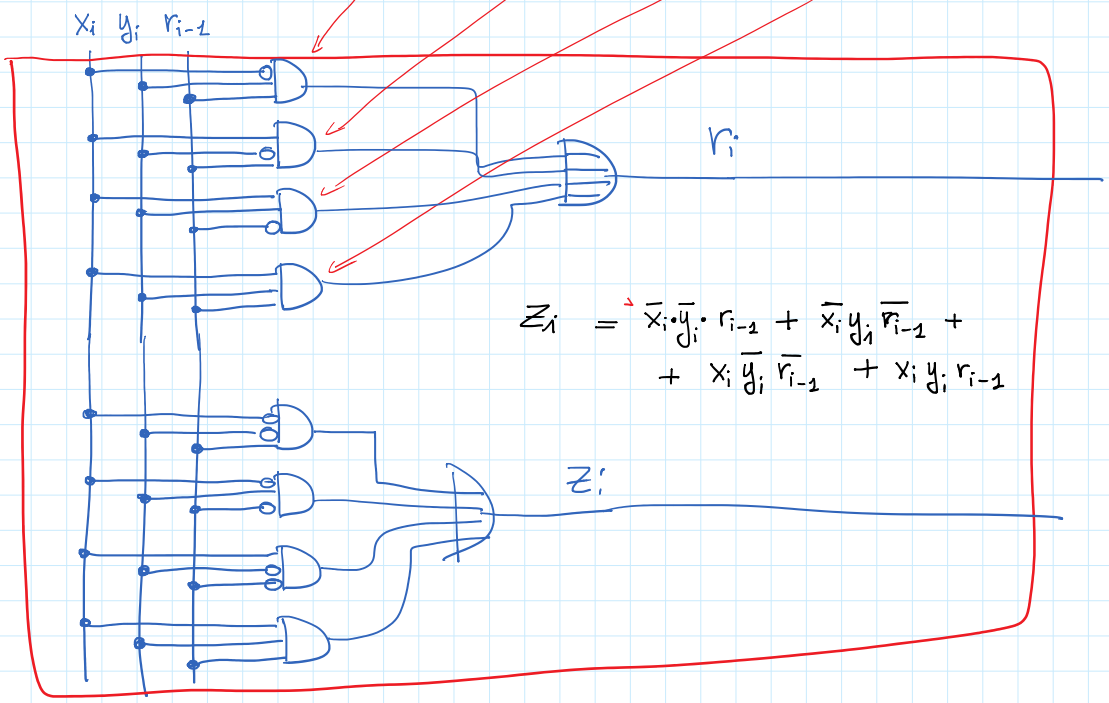


$z = 1$ sse $\forall x_i = 1$ $z = 1$ sse $\exists i \; x_i = 1$ $z = \bar{x}$ $z = x_1 \bar{x}_2$

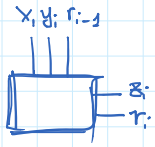


$z = \overline{x_1 x_2}$

$$r_i = \bar{x}_i y_i r_{i-1} + x_i \bar{y}_i r_{i-1} + x_i y_i \overline{r_{i-1}} + x_i y_i r_{i-1}$$

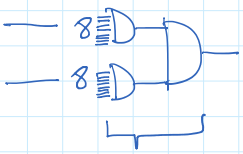


$$z_i = \bar{x}_i \bar{y}_i r_{i-1} + \bar{x}_i y_i \overline{r_{i-1}} + x_i \bar{y}_i \overline{r_{i-1}} + x_i y_i r_{i-1}$$



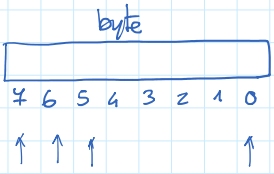
Porte max 8 ingressi introduce un ritardo (tempo) t_p

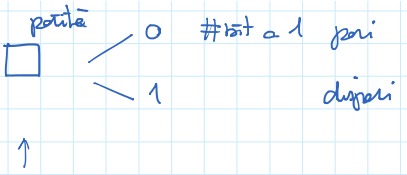
AND (16 ingressi)

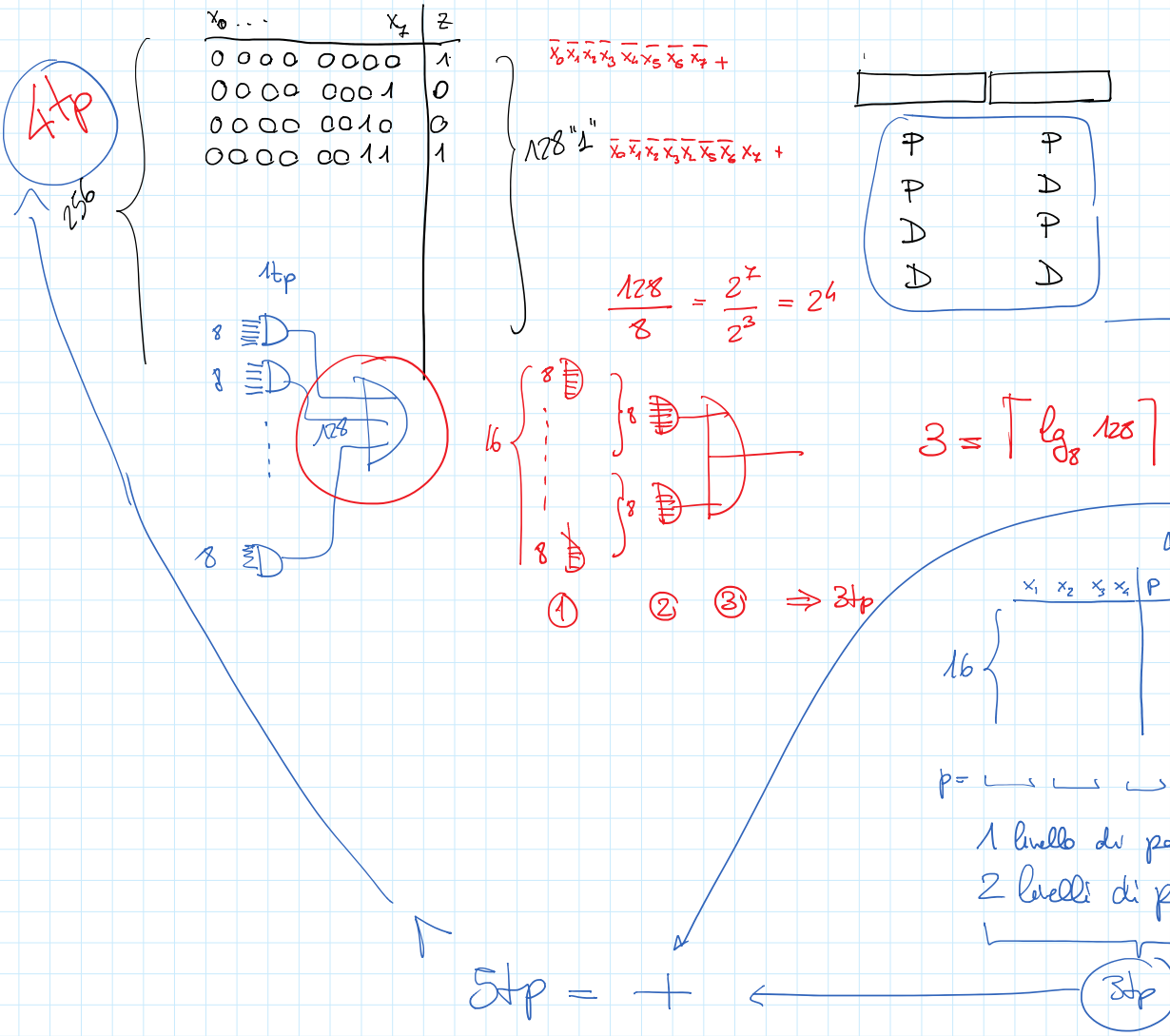


2 livelli di porte $\Rightarrow$ $2t_p$

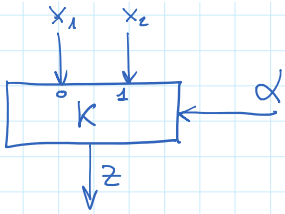
Parità


byte
7 6 5 4 3 2 1 0


parità
0 #bit a 1 pari
1 dispari


4tp
256
1tp
128
8
$\frac{128}{8} = \frac{2^7}{2^3} = 2^4$
16
$3 = \lceil \log_8 128 \rceil$
OR 2 "1"
AND 2 ingressi
2tp
1 2 3 ⇒ 3tp
8 "1"
p =
1 livello di porte AND (And a 4 ingressi)
2 livelli di porte OR (OR da 16 ingressi)
3tp
5tp = +

Commutatore



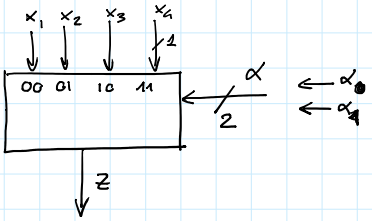
se $\alpha=0$ then $z = x_1$
else $z = x_2$

x_1	x_2	α	z
0	0	0	0
0	0	1	0
0	1	0	0
0	1	1	1 ←
1	0	0	1
1	0	1	0
1	1	0	1
1	1	1	1

α	x_1	x_2	z
0	1	–	1
0	0	–	0
1	–	0	0
1	–	1	1

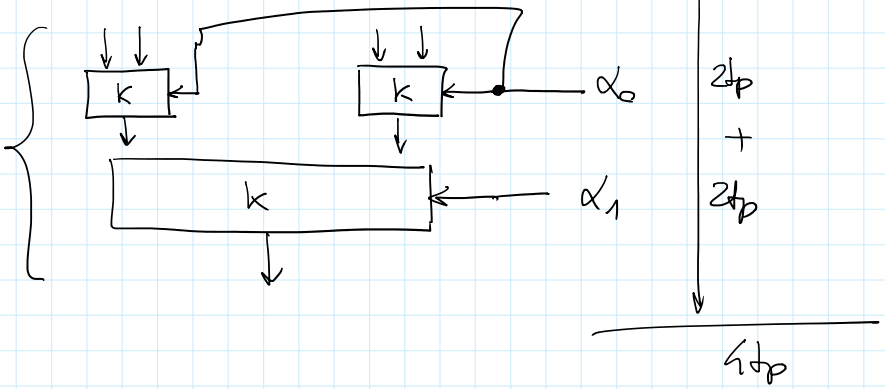
$z = \bar{\alpha} x_1 + \alpha x_2$

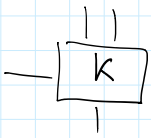
$z = \bar{x}_1 x_2 \alpha + x_1 \bar{x}_2 \bar{\alpha} + x_1 x_2 \bar{\alpha} + x_1 x_2 \alpha$

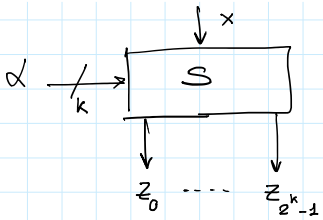


α_0	α_1	x_1	x_2	x_3	x_4	z
0	0	1	–	–	–	1
0	1	–	1	–	–	1
1	0	–	–	1	–	1
1	1	–	–	–	1	1

$z = \bar{\alpha}_0 \bar{\alpha}_1 x_1 + \bar{\alpha}_0 \alpha_1 x_2 + \alpha_0 \bar{\alpha}_1 x_3 + \alpha_0 \alpha_1 x_4$







α	X	z_1	z_2
0	1	1	0
1	1	0	1

α_0	α_1	X	z_1	z_2	z_3	z_4
0	0	1	1	0	0	0
0	1	1	0	1	0	0
1	0	1	0	0	1	0
1	1	1	0	0	0	1
0	0	0	0	0	0	0
0	1	0	0	0	0	0
1	0	0	0	0	0	0
1	1	0	0	0	0	0

selezionatore

$z_i = 0 \quad \forall i \neq \alpha$

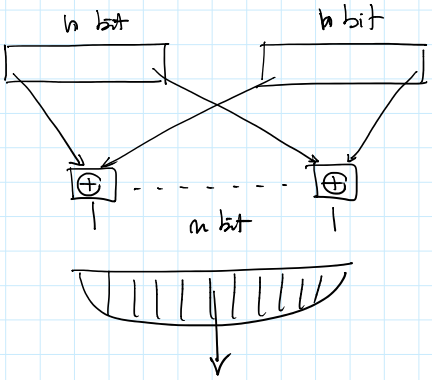
$z_i = X \quad i = \alpha$

confrontatore

$z = 0$ sse $x_1 == x_2$
altrimenti $z = 1$

x_1	x_2	z
0	0	0
0	1	1
1	0	1
1	1	0

$z = x_1\bar{x}_2 + \bar{x}_1 x_2$



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