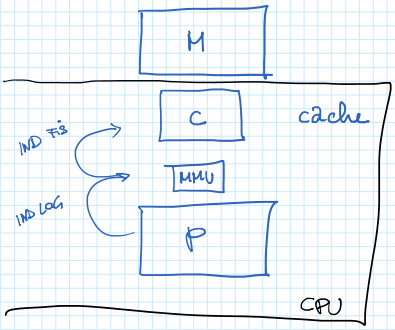
CACHE

mercoledì 16 novembre 2016 14:13

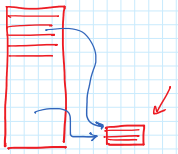


$dim(M) >> dim(C)$

$O(Gb)$ $O(K) - O(M)$

$ta_M >> ta_C$

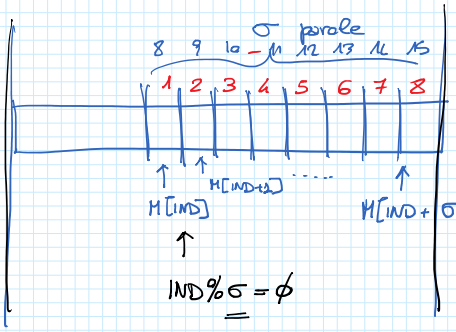
10msec nsec



modalità di indirizzamento delle memorie cache

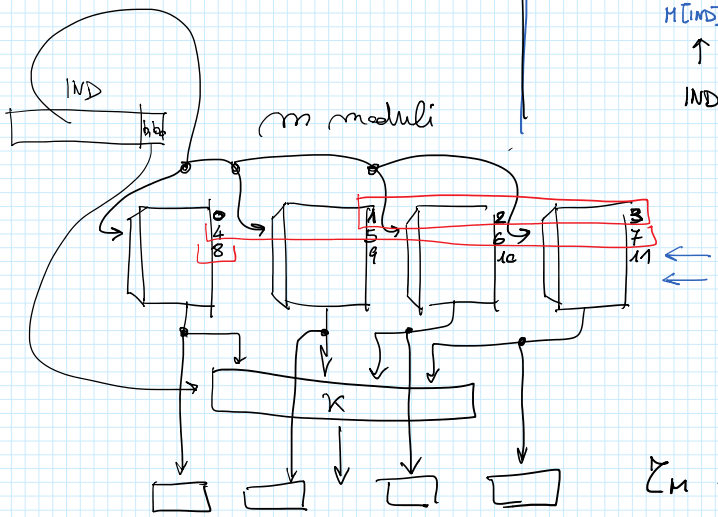
- diretto
- completamente associativo
- associativo su insiemi (set associative)

linea (blocco)



presa da un'area di M contigua

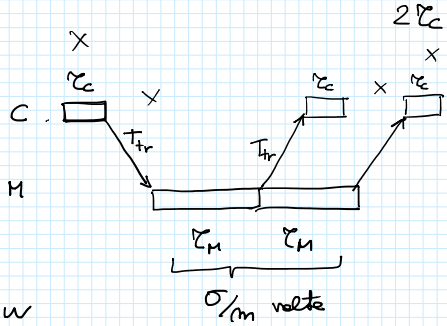
$IND \% \sigma = \phi$

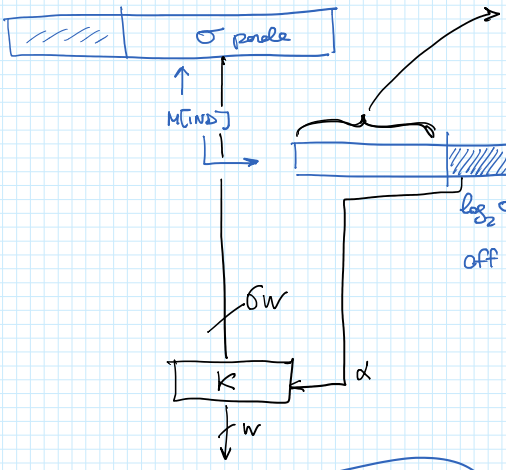


$\tau_M \rightarrow 4w$

$M \xrightarrow{\sigma} C$

$2\tau_c + 2T_{tr} + \frac{\sigma}{m}\tau_M$

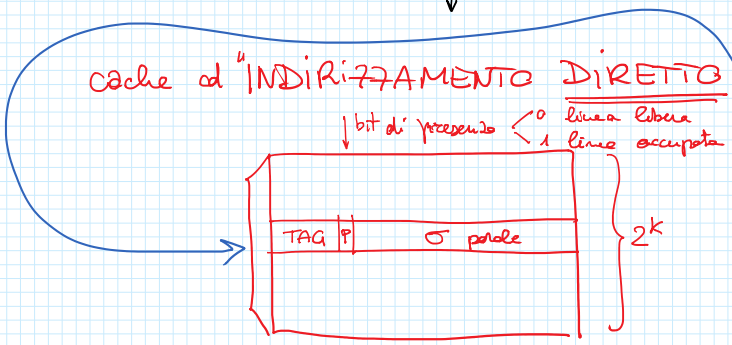




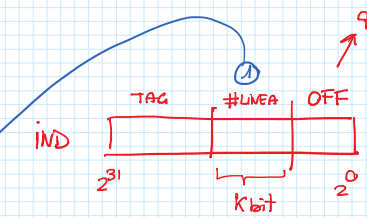
1° scopo → capire in quale linea di cache vado a cercare (se c'è) la parola di indirizzo IND

2° scopo → capire se nella linea di cache individuata c'è la porzione di M che sto veramente cercando

cache ad "INDIRIZZAMENTO DIRETTO"



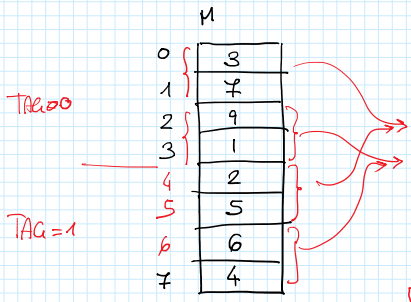
Capacità complessiva: $\sigma \cdot 2^k$ parole



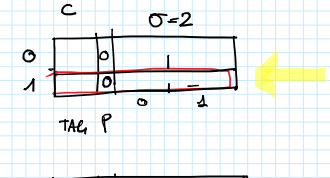
procedura logica x leggere nella cache la parola di indirizzo IND

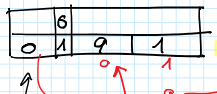
1) vado nella linea di ind #linea
2) controllo che P=1 e che IND.TAG = C[#LINEA].TAG
   - vero / falso
3) uso IND.OFF per prendere la parola che cerco

fault di cache



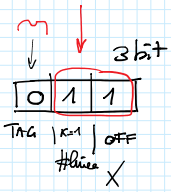
C σ=2 #linee=2 k=1





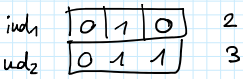
LOAD R_b, R_i, R_1

LOAD → ind = 3



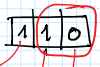
INC R_1

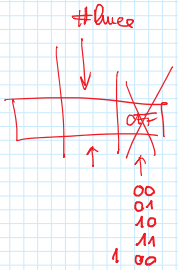
STORE R_b R_i R_1



FALSO

LOAD → ind = 6

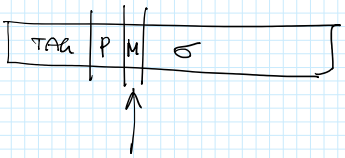




GESTIONE

mercoledì 16 novembre 2016 15:15

$P \xrightarrow{MMU} C$ ind { da leggere / da scrivere



bit di modifica

a) quando carico da M lo metto a ϕ

b) ogni volta che scrivo (una delle σ parole) lo metto a 1

1) Cerco a) identifico #linea
b) controllo P=1
c) controllo TAG =

2) se l'ho trovato → eseguo l'operazione < LOAD / STORE

2.1) se non l'ho trovato (fault di cache)

↳ trovare la posizione in cui l'avrei cercato

Vedere se la linea #linea è occupata

P=0

ordino la lettura delle σ parole della M in C

eseguo operazione LOAD STORE

P=1

controllare una delle σ parole è stata modificata

M=1 SÌ

Salvare i dati modificati in M

M=0 NO

FIRMWARE

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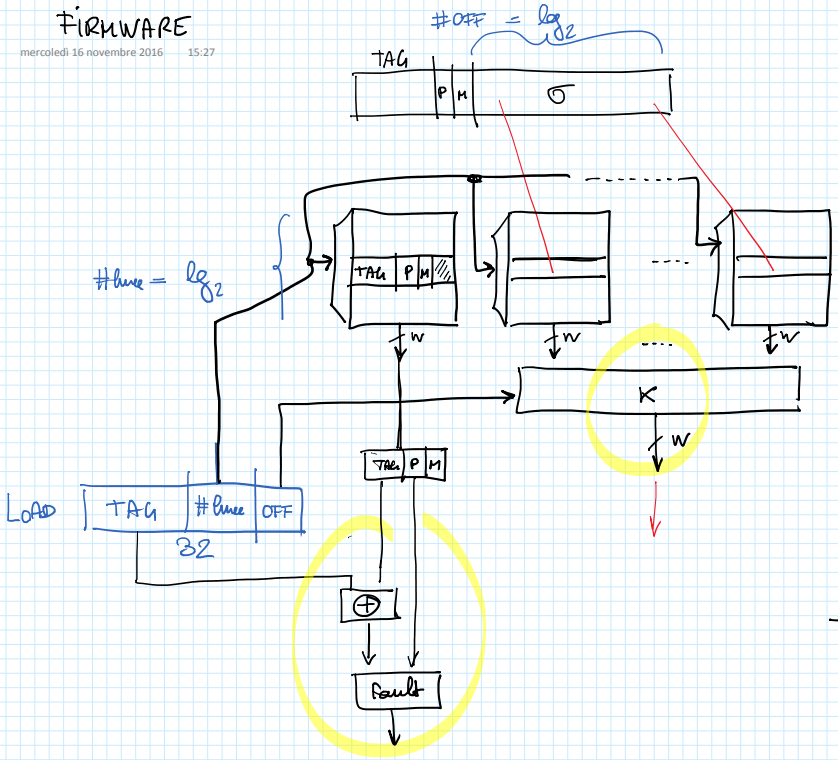
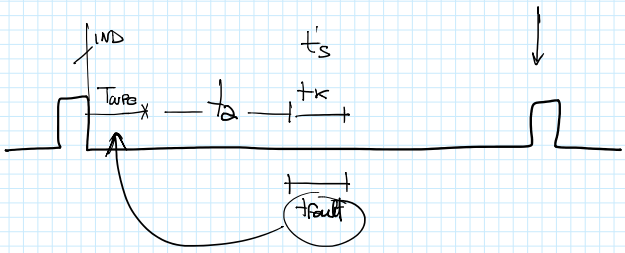




$\emptyset$. (FAULT (IND) = 0)

M[OFF][~~# linea~~] →

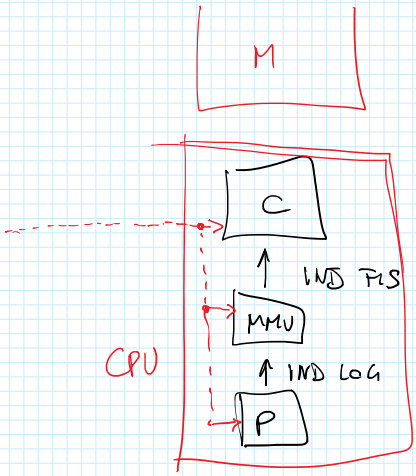
⟹ cache lavora in 1 τ

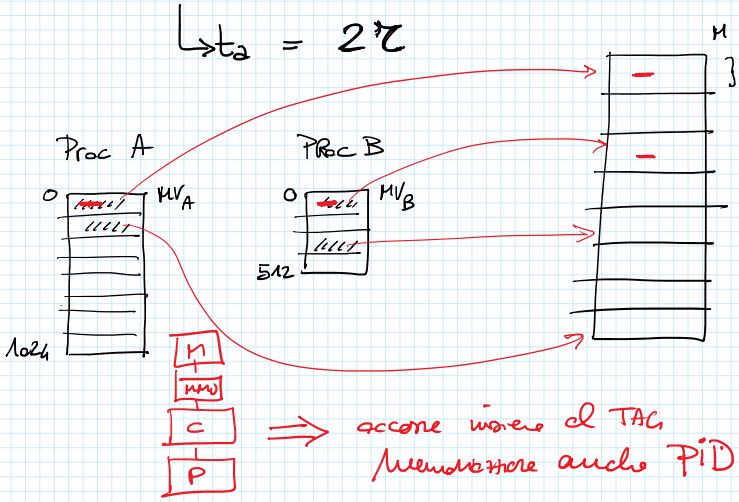
+

1 τ × MMU

in assenza di fault di cache

↳ $t_2 = 2\tau$





⟹ accesso inviato al TAG
memorizzato anche PID

COMPLETAMENTE ASSOCIATIVO

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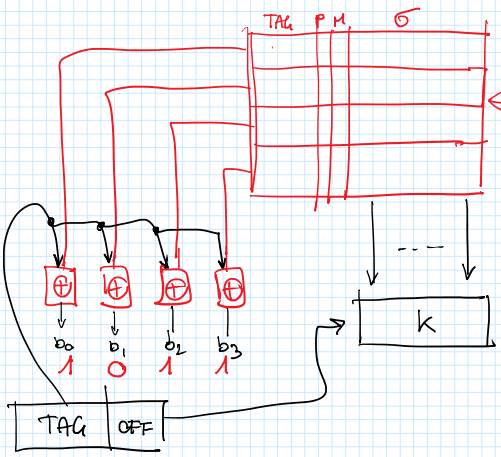


$AND(b_0, b_1, b_2, b_3)$ — 0 — 1

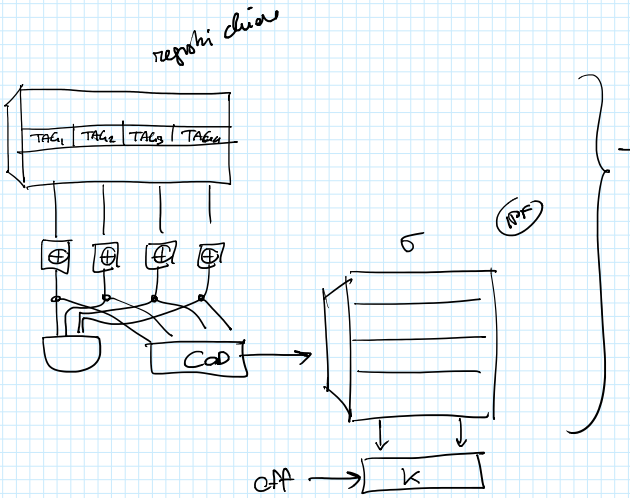
∃ pos con il TAG giusto

Fault di cache

b_0	b_1	b_2	b_3	i_1 i_2
0	1	1	1	0 0
1	0	1	1	0 1
1	1	0	1	1 0
1	1	1	0	1 1

COD

indirizzo dove cercare la σ perché ha modi scegliere con OFF



t_2 accesso a tag e fault

t_2 accesso σ

2τ

+

MMU

$3\tau = t_2$