

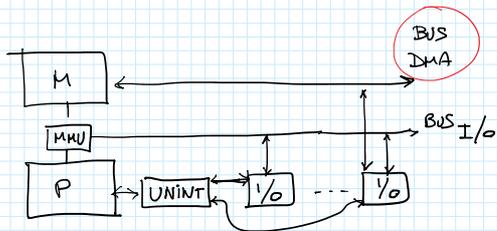
I/O

venerdì 25 novembre 2016 13:36

UNITA' I/O

- A CARATTERE: mouse, tavoletta grafica, joystick
- A BLOCCHI: disco, int di rete

10 msec -3 msec -3 msec

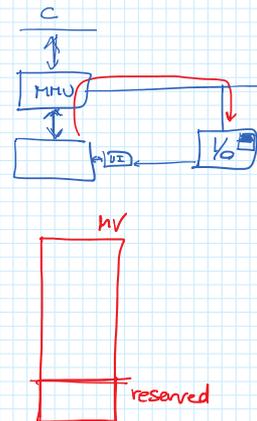
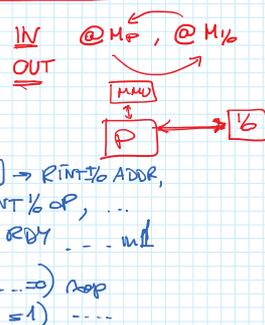
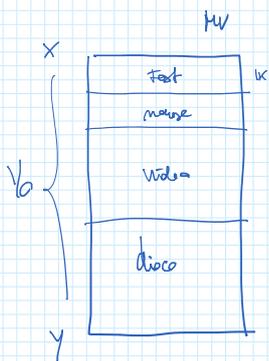


TRASFERIMENTI DEI DATI (fra P/m e I/O)

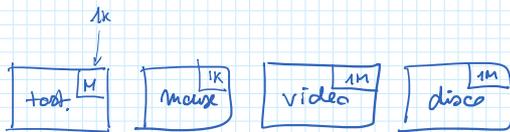
MODELLI (dal punto di visto ASM)

MEMORY MAPPED I/O

ISTRUZIONI SPECIALI

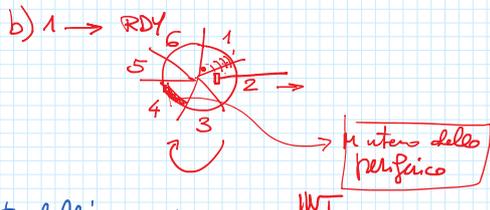


a) stato con + il comando da eseguire nello periferico + i suoi parametri



nello MV che rappresenta lo memoria dell'unita di I/O

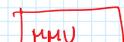
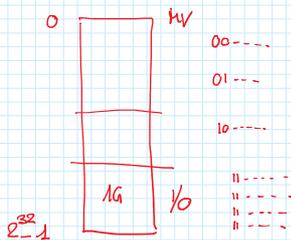
a) so. leggi il settore 4 della traccia 1
↳ op e param → bc M16



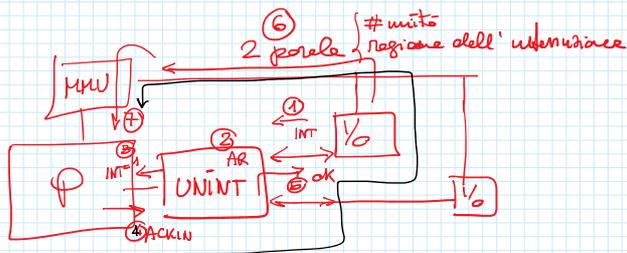
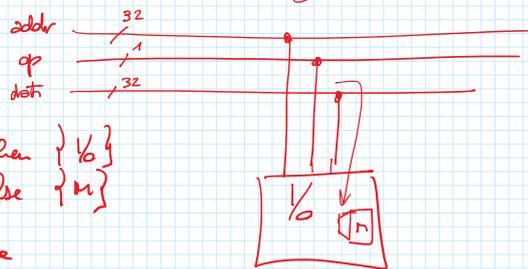
b) ordinare l'esecuzione del comando
store #1 → "RDY" della periferico

c) attenda un'interruzione

d) quando arriva ⇒ LOAD dallo memoria di I/O per leggere il risultato dell'operazione



if (ind == 11xxx) then { I/O } else { M }



fase
firmware
del
trattamento
int

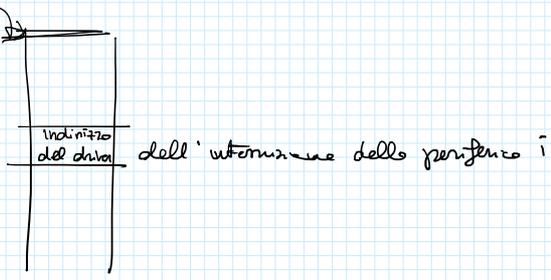
tratt_int. reset INT, set ACKINT, tratt_int1
tratt_int1. (ACK_m = 0) map, tratt_int1
(=1) DATAIN → REG[61], reset ACK_m, set RDM_m, tratt_int2
tratt_int2. (ACK_m = 0) map, tratt_int2,
(=1) DATAIN → REG[62], IC → REG[63], set RDM_m, reset ACK_m, REG[60] → IC, chip

costo TRATT_INT_ASH

DRISC
OSM

da qui in poi è la
fase assembler
(del trattamento delle
indennità)

R(Tab-int)
vettore di interruzione



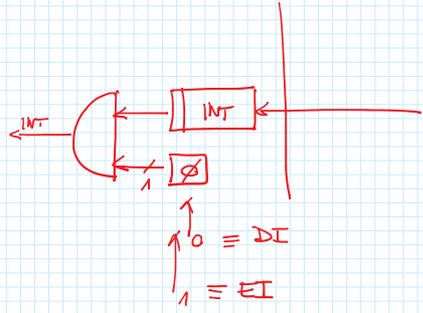
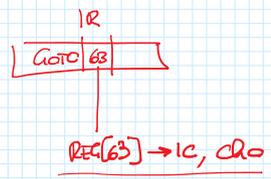
```
LOAD Rtab-int, R61, Rhandler, DI
CALL Rhandler, Rret
→ GOTO R63, EI
```

disable interrupt

← deve essere veloce > che

enable interrupt

cho
chis
getop



```
"op-ultima" → M[IND-1/6-DISCO];
#naccia → M[IND-1/6-DISCO+1];
#settore → M[IND-1/6-DISCO+2];
1 → M[IND-1/6-DISCO+OFFSET];
```

commutazione di contesto

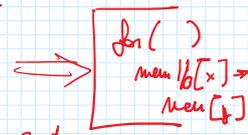
DRIVER

hott-int

2

INT

```
LOAD ,DI
CALL
```

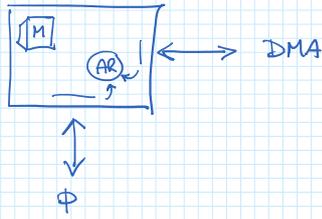


GOTO Rret

DMA (I/O)

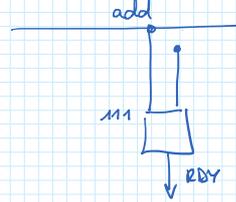
venerdì 25 novembre 2016 15:47

direct memory access



DMA + MM I/O x disco

- a) memoria op e parametri via MM I/O nello periferica
- b) memoria "GO" nel RBY dello periferica



c) ottendo INT

fine

I/O completo op
accede bus DMA
e esegue il ciclo di trasferimento
M ↔ M/I/O
scatenando un'interruzione