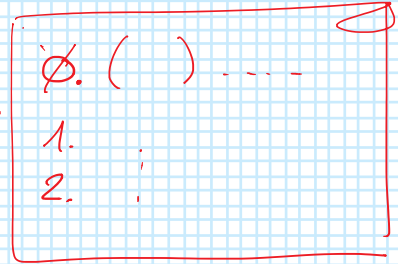
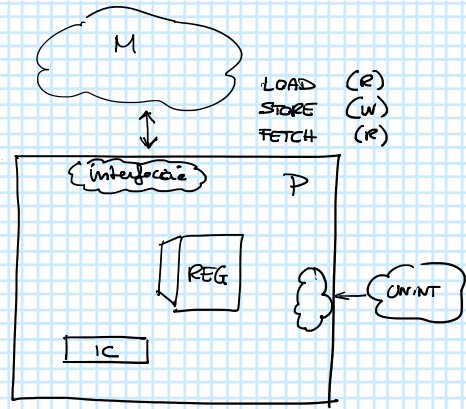
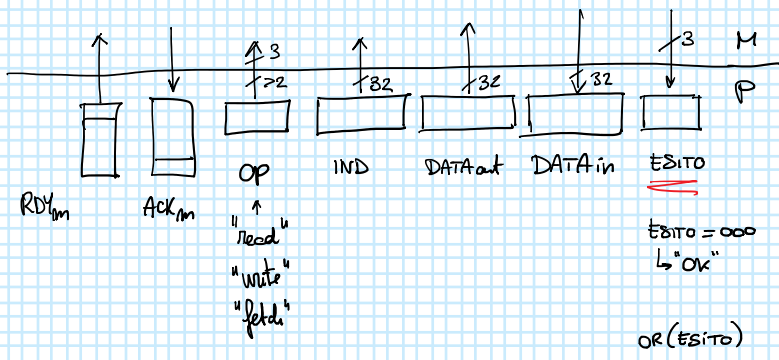


```

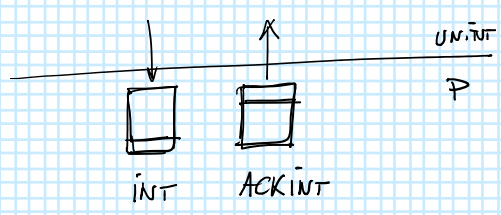
while (true) {
    fetch ISTR (IC PC)
    decode ISTR
    exec ISTR
    trattamento informazioni
}
    
```



INTERFACCIA verso M

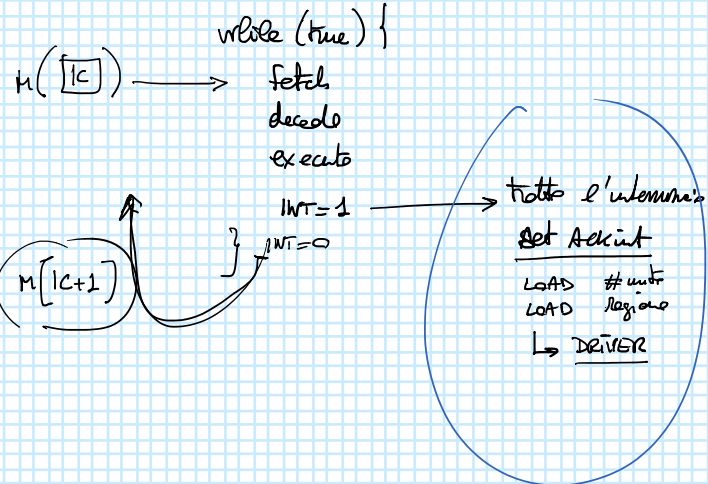


INTERFACCIA verso UNINT



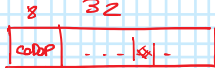
$\emptyset.$  richiama a M la lettera M[IC]

- obtiene la lettera
    - switch (pop)
- Case "ADD": 2. ...  
 Case "SUB": 3. ...  
 Case "LOAD": 4. (INT=0) ...  $\emptyset$



IR instruction register

IR.COP  
 IR.REGA IR.REGB IR.REGC  
 IR.OFFSET



∅. "fetch" → OP, IC → IND, set RDY<sub>m</sub>, 1.

1. (ACK<sub>m</sub>, DR(ESITO) = 0 - ) map, 1

(= 10) DATA IN → IR, reset ACK<sub>m</sub>, 2  
 (= 11) ..., hanteccazioni

2. (IR.COP, INT = "ADD", 0)

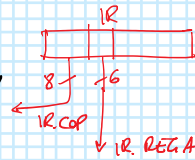
$REG[IR.REGA] + REG[IR.REGB] \rightarrow REG[IR.REGC]$

IC + 1 → IC, ∅

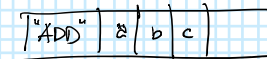
(= "ADD", 1)

$REG[IR.REGA] + REG[IR.REGB] \rightarrow REG[IR.REGC]$

IC + 1 → IC, halt int



IR.COP  
 IR[0..7]  
 IR.REGA  
 IR[8..13]



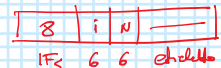
↑ indizio di una parte di μ-codice che realizza il hanteccamento dell' int

(= "LOAD", 0) "read" → OP, REG[IR.REGA] + REG[IR.REGB] → IND, set RDY<sub>m</sub>, reset ACK<sub>m</sub>,

LOAD R<sub>base</sub>, R<sub>index</sub>, R<sub>dest</sub>  
 $R[R[base] + R[index]] \rightarrow R[dest]$

(= "IF<", 0)  $SEGO (REG[IR.REGA] - REG[IR.REGB]) \rightarrow S, 4$

IF< R<sub>i</sub>, R<sub>N</sub>, loop



3. (ACK<sub>m</sub>, DR(ESITO) = 0 - ) map, 3

(= 100) DATA in → REG[IR.REGC], reset ACK<sub>m</sub>, IC + 1 → IC, ∅

(= 101) " " " " " , halt int

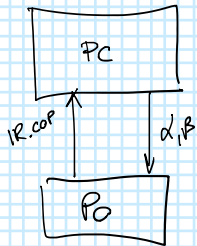
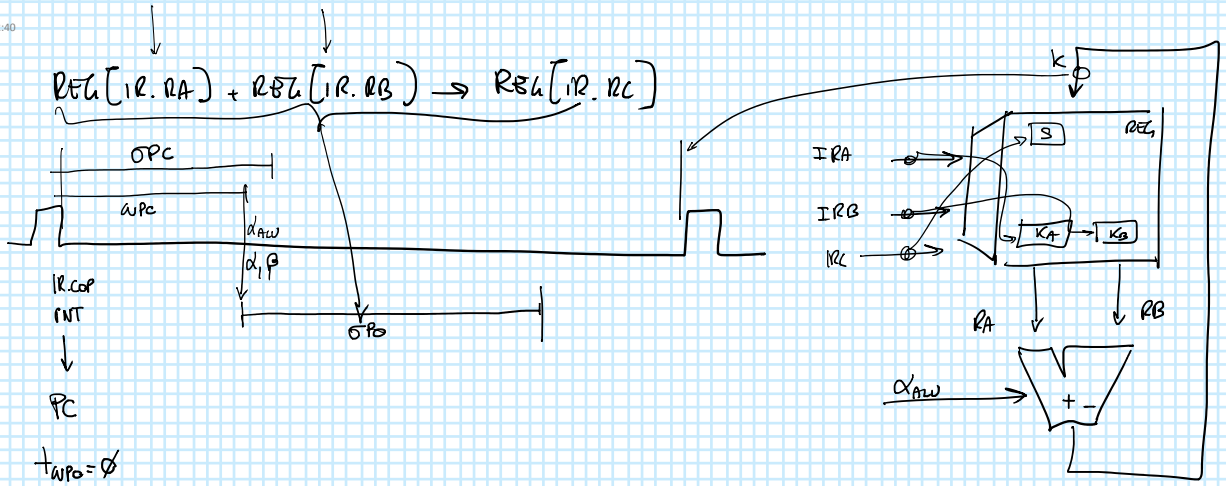
(= 11-) " " " " " , hanteccazioni

4. (S, INT = 1 ∅) IC + IR.chiaveto → IC, ∅

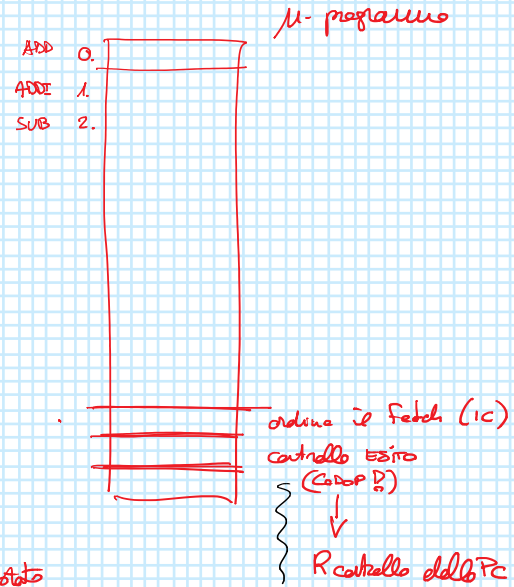
(= 11) IC + IR.chiaveto → IC, hanteccazioni

(= 00) IC + 1 → IC, ∅

(= 01) IC + 1 → IC, hanteccazioni



ADD	0
ADDI	1
SUB	2
...	...
LOAD	15
...	...



chp. "fetch" -> op, IC -> IND, set RDYm, chl

chl. (ACK<sub>m</sub>, alpha(ESITO) = phi -) nop, chl  
 (= 10) DATA IN -> IR, ~~IR.cop~~ -> RC  
DATA IN.cop

aggiornamento di stato dello PC (# istruzioni che eseguiranno immediatamente dopo)

addp. (INT=0) REG[IR.RA] + REG[IR.RB] -> REG[IR.RC], IC+1 -> ic, chl  
 (=1) " " " " , halt int

subp. (INT=0) REG[IR.RA] - REG[IR.RB] -> REG[IR.RC], IC+1 -> ic, chl  
 (=1) " " " " , halt int

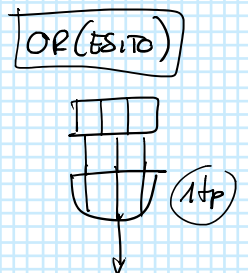
loadp. "read" -> op, REG[IR.RA] + REG[IR.RB] -> IND, set RDYm, load1

load1. (ACK<sub>m</sub>, OR(ESITO), INT = 0 --) nop, load1  
 (= 100) DATA IN -> REG[IR.RC], IC+1 -> ic, chl  
 (= 101) " " " " , halt int  
 (= 11-) halt eccezioni

ESITO<sub>0</sub> ESITO<sub>1</sub> ESITO<sub>2</sub> = 000

IR 0. segue (REG[IR.RA] - REG[IR.RB]) -> S, IR 1

IR 1. (S, INT = 10) IC + IR. etichetta -> IC, chl  
 (= 11) " " " " , halt int  
 (= 00) IC+1 -> IC, chl  
 (= 01) " " " " , halt int



(= m)  
(= 00)  
(= 01)

lc+1 → lc , <sup>new un</sup> ~~clp~~  
" , realt. unt

