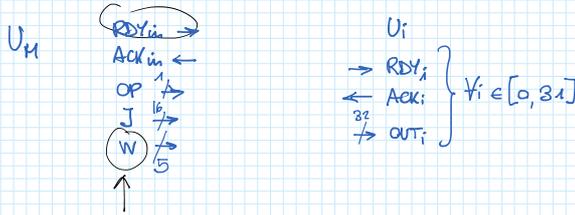


OP=0
 $A[i] = B[i]$
 \neq
 OP=1
 $A \leftrightarrow B$
 $\forall i: A[i] \leftrightarrow B[i]$

$$\frac{A[j] + B[j]}{64}$$

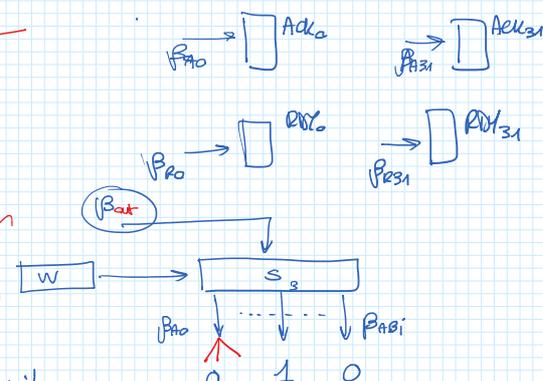
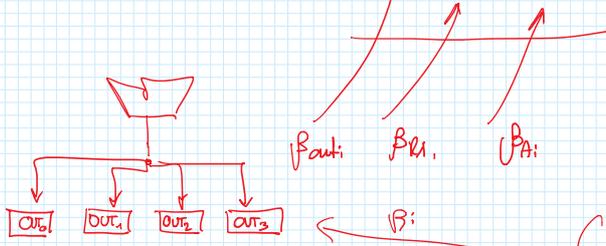
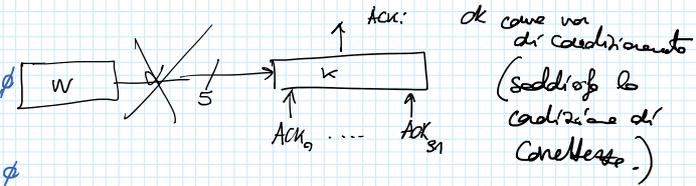
$$\frac{A[j] - B[j] \% 128}{}$$

A, B CLK
 32bit



$\emptyset. (RDY_{in}^{OP} = \emptyset) \text{ map, } \emptyset$
 $(=10)$
 $RDY_{in}, OP, \text{ zero}(A[i] - B[j])$
 $\rightarrow OUT_i$

$\emptyset. (RDY_{in}, OP, \text{ zero}(A[i] - B[j]), ACK_i = 0) \text{ map, } \emptyset$ *attesa di U_n*
 $(=1001)$
 $(A[i] + B[i]) / 64 \rightarrow A[i]$
 $(A[i] + B[i]) / 64 \rightarrow OUT_i$
 Reset RDY_in, set ACK_in, set RDY_i, reset ACK_i, \emptyset
 $(=1011)$
 $(A[i] - B[i]) \% 128 \rightarrow A[i]$
 $(A[i] - B[i]) \% 128 \rightarrow OUT_i$
 Reset RDY_in, set ACK_in, set RDY_i, reset ACK_i, \emptyset



$(=10-0)$ map, \emptyset *attesa di U_i*
 $(=11--)$ $0 \rightarrow I, 1$
 1. $(I_0 = 0) A[i] \rightarrow B[i], B[i] \rightarrow A[i]$
 $I+1 \rightarrow I, 1$
 $(=1)$ set ACK_in, reset RDY_in, \emptyset
 map

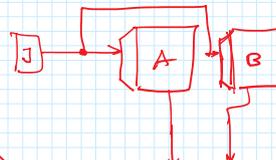
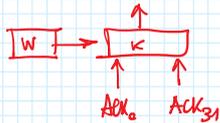
$I = 17 \text{ bit}$
 I_m

Vale la condizione di correttezza?

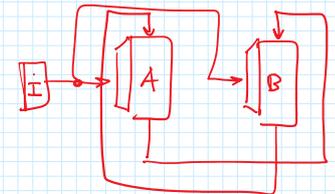
occorre stabilire che:

- ✓ RDY_{in}
- ✓ OP
- ✓ zero (A[J] - B[J])
- ✓ ACK:

nessun altri valori che dipendono dal solo stato interno dello P0

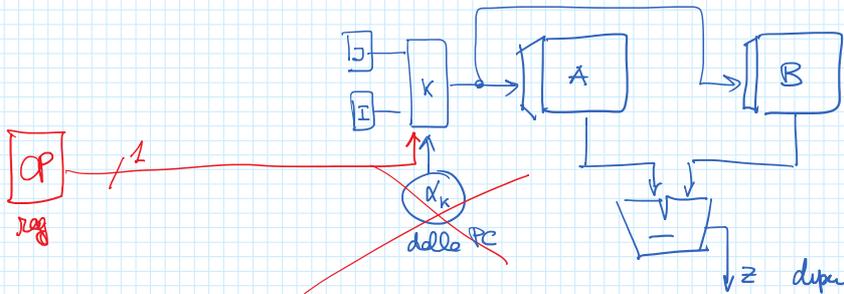


$$A[i] \rightarrow B[i], B[i] \rightarrow A[i]$$



lor di cond.

Sol 1



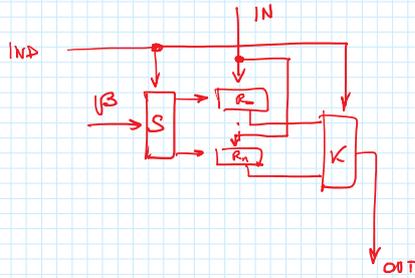
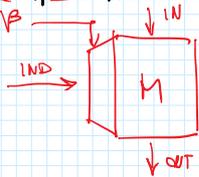
altro soluzione **Sol 2**

$$\text{zero}(A[J] - B[J]) \rightarrow z, 1$$

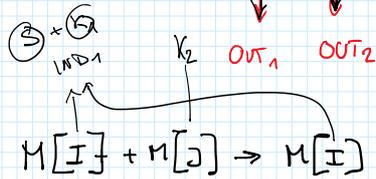
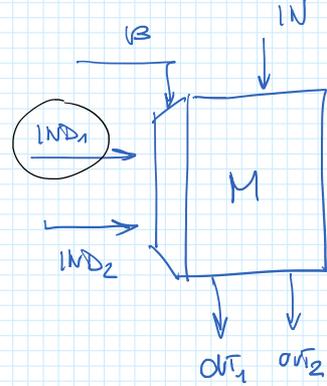
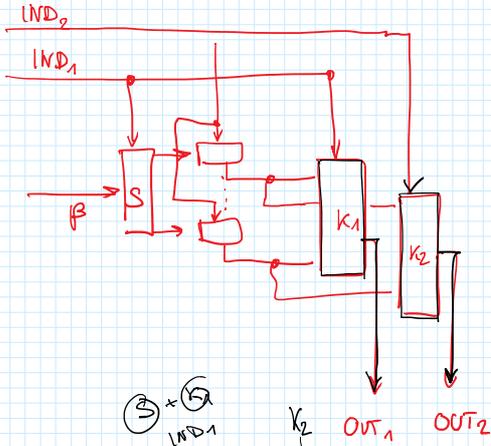
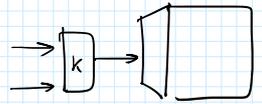
1. (z=0) ---
- (z=1) ---

0. (RDY, OP = 0-) nop
 (= 11) 0 → I, 1
 (= 10) zero(A[J] - B[J]) → z, 2
1. (I₀ = 0) A[I] → B[I], B[I] → A[I], I+1 → I, 1
 (= 1) set ACK_{in}, reset RDY_{in}, 0
2. (z, ACK_{in} = 01) A[J] - B[J] % 128 → OUT_i, A[J]
 (= 11) A[J] + B[J] / 64 , 0
 (= -0) nop, 2

memorie a doppie porte



memoria standard



con 3 utilizări (1 x K1, 1 x K2, 1 x S)
 $M[I] + M[J] \rightarrow M[k]$



Ø. (RDY, OP = Ø-) nop.

(= 11) Ø → I, 1

(= 10) zero (A[J] - B[J]) → Z, 2

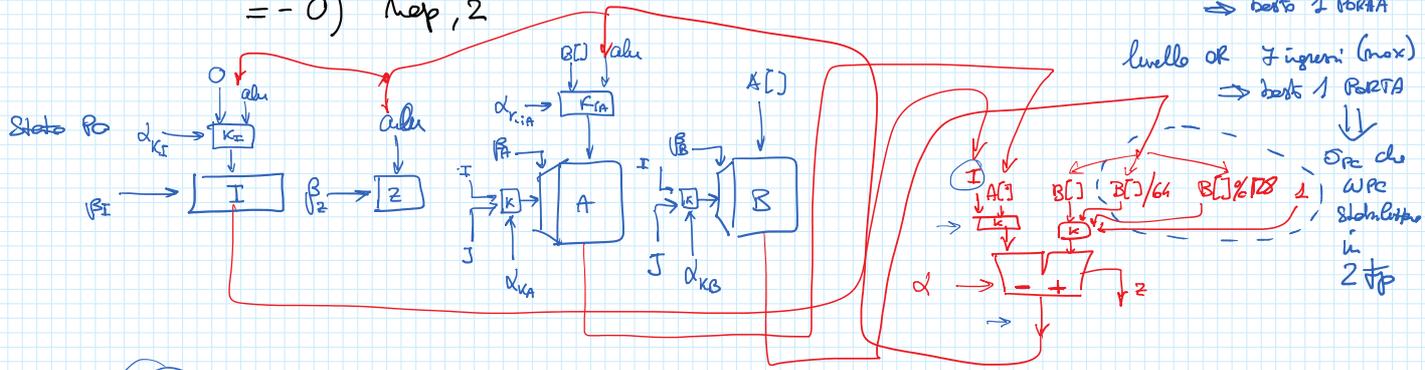
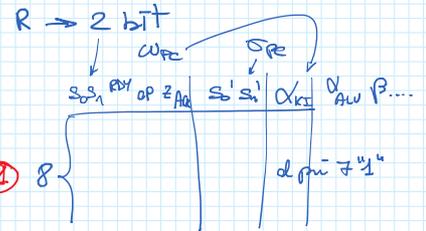
1. (I₀ = 0) A[I] → B[I], B[I] → A[I], I+1 → I, 1

(= 1) set ACK_i, reset RDY_i, Ø

2. (Z, ACK_i = 01) A[J] - B[J] % 128 → OUT_i, set ACK_i, reset RDY_i, reset ACK_i, Ø

(= 11) A[J] + B[J] / 64

= -0) nop, 2



livello AND 6 ingressi → porta 1 PORTA

livello OR 7 ingressi (max) → porta 1 PORTA

Ø se che WPC stabilizza in 2 fp

ω_{PC} σ_P
 RDY, OP, Z ⇒ ϕ_{tp}
 ACK_i ⇒ t_{K32} } ?

$T_{WPC} = t_{K32}$

$T_{OP} = t_a + t_k + t_{cu}$?

