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www.di.unipi.it/~marcod

342

mercoledi 9.30 12.30

logica booleana sistema binario
reti logiche
microarchitettura + assembler (ARM v7 v8)
memoria
I/O

(VHDL)
Verilog

iverilog
gtkwave

(quartus)

FPGA — ALTERA → INTEL
XILINX

ASM ARM

.asm → VISUAL / GNU → .exe

① cross compiler
- qemu -arm
- gdb

② gdb

'80 6502 Z80 8088

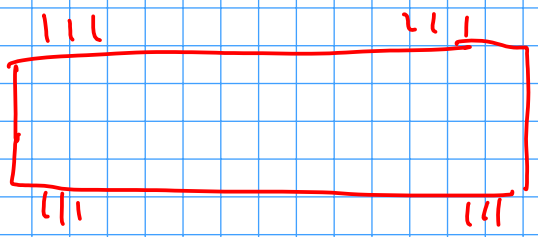
Apple II 16 bit

Z80

8 bit

ACCUMULATORE

1 MHz



Moore

architetture

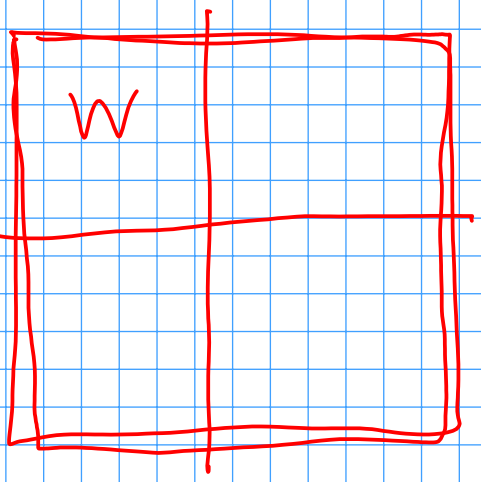
tecnologia

10nm

6-7nm

super pipeline

super scalari



dark sylicon

GPU

multicore

Xeon

16-24 core

(2 thread x core)

2-3 GHz

Phi

KNC

KNL

60-64 (4 thread x core)

1 GHz

N Atom

10x

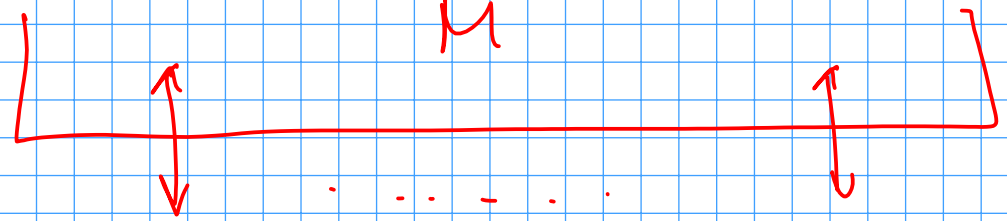
1) porte logiche

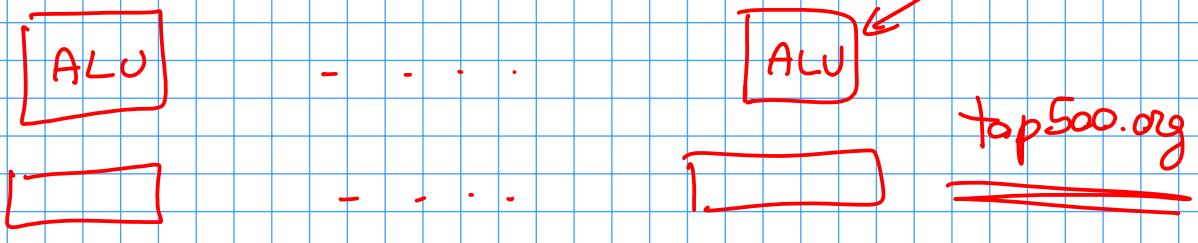
2) reti comb + seq

3) asm → μ architettura

- 1 istruzione alla volta
- pipeline
- superscalare
- multicore

GPU (SIMD)





top500.org

E

PFLOPS

MIPS

FLOPS/W